A SOLECTRON COMPANY

PPC/PowerCoreCPCI-6750

Reference Guide

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Table of Contents

List of Tables and Figures

Using This Manual

This section does not provide information on the product but on common features of the manual itself:

- its structure,
- special layout conventions,
- and related documents.

Audience of the Technical Reference Manual

The *Technical Reference Manual* is intended for hard- and software developers installing and integrating the PPC/PowerCoreCPCI-6750 into their systems.

Overview of the Technical Reference Manual

The *Technical Reference Manual* additionally includes the *PowerBoot User's Manual*.
The *Technical Reference Manual* provides a comprehensive hardware and software guide to the board.

IMPORTANT

Please take a moment to examine the "Table of Contents" of the *Technical Reference Manual* to see how this documentation is structured. This will be of value to you when looking for information in the future.

Technical Reference Manual

The *Technical Reference Manual* includes:

- a brief overview of the product, the specifications, and the ordering information: see section 1 "Introduction" on page 1.
- the installation instructions for powering up the board: see section 3 "Installation" on page 9. It includes the default configuration (switches and the like), initialization, and connector pinouts.

  The installation instructions also appear as the product's installation guide – a separate manual delivered together with each shipped product.
- a detailed hardware description: see section 3 "Hardware" on page 25.

- a description of the board specific PowerBoot commands: see section 5 “PowerBoot for PPC/PowerCoreCPCI-6750” on page 81.

PowerBoot User’s Manual

The *PowerBoot User’s Manual* describes only those PowerBoot commands which are independent of the board. The board specific PowerBoot commands are described in the *Technical Reference Manual* (see section 5 “PowerBoot for PPC/PowerCoreCPCI-6750” on page 81).
The *PowerBoot User’s Manual* is packaged separately and always shipped together with the *Technical Reference Manual*.

☞ **Insert the *PowerBoot User’s Manual* now: see section 4 “PowerBoot (= PowerBoot User’s Manual)”.**

Publication History of the Manual

Table a **History of Manual Publication**

Edition/ Revision	Date	Description
1.0	July 1998	First print
1.1	December 1998	Excerpt from the data sheet's ordering information updated, power requirements and bus frequencies of the 300-MHz and 400-MHz boards included, SETBOOT corrected, flash memory programming exemplified
2.0	April 1999	Edition increased to archive Rev. 1
3.0	April 1999	PPC/PowerCoreCPCI-6750 Rev. 2
AA	November 2000	Added safety notes; editorial changes; removed data sheets
AB	August 2001	Added chapter Sicherheitshinweise
AC	August 2002	Editorial changes

Fonts, Notations and Conventions

Table b **Fonts, Notations and Conventions**

Notation	Description
`0000.0000`$_{16}$	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
`0000`$_{8}$	Same for octal numbers (digits are 0 through 7)
`0000`$_{2}$	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like that should be used typing literally the same word. Also used for on-screen-output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like and that will be replaced by an applicable value when actually applied.

Table b **Fonts, Notations and Conventions (cont.)**

Notation	Description
#	A # symbol at the end of a PCI, ISA, or IDE signal name indicates that the signal is active when it is at low voltage. The absence of the # symbol indicates that the signal is active at high voltage.
*	A * symbol at the end of a VMEbus signal name indicates that the signal is active when it is at low voltage. The absence of the * symbol indicates that the signal is active at high voltage.

Register Conventions

Force Computers assumes that the software developer initializes the register bits which are not described with default settings.

Icons for Ease of Use: Safety Notes and Tips & Tricks

There are 3 levels of safety notes used in this manual which are described in short in the following subsections by displaying a typical layout example.

Be sure, to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

CAUTION

Dangerous situation: injuries to people or severe damage to objects possible.

NOTICE

Possibly dangerous situation: no injuries to people but damage to objects possible.

IMPORTANT

No danger encountered. Only application hints and time-saving tips & tricks or information on typical errors when using the information mentioned below this safety hint.

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PPC/PowerCoreCPCI-6750. For your protection, follow all warnings and instructions found in the following text. This Technical Reference Manual provides the necessary information to install and handle the PPC/PowerCoreCPCI-6750. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The PPC/PowerCoreCPCI-6750 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, uninstall or maintain the PPC/PowerCoreCPCI-6750. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A.

These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The board generates, uses and can radiate radio frequency energy and, if not installed properly and used in accordance with this Technical Reference Manual, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If boards are integrated into open systems, always cover empty slots.

To ensure proper EMC shielding, always operate the PPC/PowerCoreCPCI-6750 with the blind panels or with PMC modules installed.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing or uninstalling the board, check the “Requirements” section on page -5.**
- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**

Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the CompactPCI rack and shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Hot Swap

Never install or uninstall the board in a system under hot-swap conditions unless the basic hot-swap, full hot swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components).

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMI and the possibly changed functionality of the product.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as your PPC/PowerCoreCPCI-6750. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meter.**

Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des PPC/PowerCoreCPCI-6750 zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des PPC/PowerCoreCPCI-6750. Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das PPC/PowerCoreCPCI-6750 erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls kann es dieses ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet und entspricht den Grenzen eines Klasse-A-Produktes gemäß Abschnitt 15 der FCC-Richtlinien, insbesondere EN 55022 Klasse A.

Diese Grenzen sind dafür vorgesehen, einen vernünftigen Schutz gegen störende Einflüsse bei einem Betrieb in einer kommerziellen Umgebung zu gewährleisten.

Das Board erzeugt elektromagnetische Strahlung. Wird das System un-sachgemäß installiert oder in anderer Weise als in diesem Installationshandbuch beschrieben betrieben, kann es in der Umgebung von Rundfunksendern und in Wohngegenden zu Störungen kommen. In diesem Fall ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen und die Kosten von Messungen selbst zu tragen.

Werden Boards in offene Systeme eingebaut, müssen freie Steckplätze mit einer Blende abgeschirmt werden.

Um eine ausreichende Abschirmung zu gewährleisten, darf das Board nur mit einer Blindblende oder mit einer installierten PMC-Karte betrieben werden.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt “Requirments” auf Seite 5.**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf das Front Panel, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die Compact-PCI Backplane angeschlossen ist und Strom an allen Power Pins anliegt.**

Betrieb

Während des Betriebs müssen die Umgebungs- und die Stromsversorgungsbedingungen gewährleistet sein.

Wenn das Board in Gebieten mit starker elektromagnetischer Strahlung betrieben wird, stellen Sie sicher, dass das Board auf dem Compact PCI Rack verschraubt ist und mit einem Gehäuse geschützt ist.

Es ist sicherzustellen, dass Anschlüsse und Kabel des Boards während des Betriebs nicht versehentlich berührt werden können.

Hot Swap

Einbau oder Ausbau des Boards in einem System unter Hot Swap Bedingungen darf nur dann stattfinden, wenn die grundlegende Hot Swap Plattform, die vollständige Hot Swap Plattform, oder die Hochverfügbarkeits Hot Swap Plattform benutzt wird und die Systembeschreibung ausdrücklich die geeigneten Richtlinien vorgibt.

Erweiterung

Beachten Sie den Gesamtstromverbrauch aller installierter Komponenten (siehe technische Daten der entsprechenden Komponente).

Vergewissern Sie sich, daß jeder individuelle Ausgangsstrom jedes Stromverbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe technische Daten des entsprechenden Verbrauchers).

Benutzen Sie bei der Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Ansonsten sind Sie für die Auswirkungen auf EMV und die möglicherweise geänderte Funktionalität des Produktes verantwortlich.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**

Umweltschutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

1 Introduction

The PPC/PowerCoreCPCI-6750 is a high-performance single-board computer providing a peripheral CompactPCI interface. It is based on

- the microprocessor PowerPC 750
- and on the PCI bus.

Memory

Per default the PPC/PowerCoreCPCI-6750 provides one memory module of up to 128 MByte. There are 2 types of memory modules available:

- EDO DRAM memory modules
- and SDRAM memory modules.

Depending on the memory module installed on the board, the memory capacity may be increased by installing an upper memory module on the (lower) memory module (see section 2.1.1 “Requirements” on page 5).

The secondary (L2) cache has a size of up to 1 MByte. The boot flash has a maximum capacity of 2 MByte and the on-board user flash has a maximum capacity of 8 MByte.

Interfaces

The PPC/PowerCoreCPCI-6750 includes a peripheral CompactPCI interface, PCI bus interfaces, Ethernet interface, and 2 serial I/O ports to provide full single-board computer functionality. The serial I/O ports are available at the front panel via 9-pin Micro D-Sub connectors.

CPU Speed

The PowerPC CPU runs with a minimum frequency of 233 MHz and provides cache snooping support in order to maintain cache coherency.

Real-Time Clock

A real-time clock with on-board battery backup is also available.

1.1 Specification

Table 1 Specification of the PPC/PowerCoreCPCI-6750

Processor	PowerPC 750
Shared memory	64-MByte EDO DRAM or 128-MByte SDRAM upgradable to max. 256 MByte
PMC slots	2 for 32-bit PMC modules I/Os for both PMC modules on CompactPCI connectors J4 and J5
Peripheral CompactPCI interface	PCI-to-PCI bridge
PCI interface	PPC-to-PCI bridge
Ethernet interface	Ethernet controller 10Base-T or 100Base-Tx on front panel, self-negotiating
2 serial I/O ports	RS-232 compatible I/O on front panel
Counters/timers	Three 16-bit, programmable
Boot flash	Up to 2 MByte On-board programmable Hardware write protection
User flash	Up to 8 MByte On-board programmable Hardware write protection
RTC/SRAM/battery	Real-time clock and NVRAM
Additional features	Reset and abort key, status LEDs, user LEDs, serial PROM for board configuration, voltage sensors, watchdog timers
Firmware	PowerBoot
Power consumption	see section 2.1 “Installation Prerequisites and Requirements” on page 5
Environm. conditions	see subsection ‘Environmental Requirements” on page 8 and table 7 “Environmental Requirements of the PPC/PowerCoreCPCI-6750” on page 8
Standards compliance	CompactPCI Specification PICMG 2.0 R2.1 CompactPCI Hot Swap Specification PICMG 2.1 R1.0 PCI Local Bus Specification Rev. 2.1 IEEE P1386.1/Draft 2.0 - Layers for PCI Mezzanine Cards: PMC

The PPC/PowerCoreCPCI-6750 is available in several memory and speed options. Consult your local sales representative to confirm availability of specific combinations.

1.2 Product Nomenclature

Table 2 Nomenclature of the PPC/PowerCoreCPCI-6750

PPC/PowerCore-6750/yyS-ccc-Llll-z	
750	PowerPC processor type 750
yyS	DRAM size in MByte, *S* means SDRAM
ccc	Processor clock frequency in MHz
Llll	L2 cache capacity in KByte
z	User flash capacity in MByte

1.3 Ordering Information

The following table is an excerpt from the PPC/PowerCoreCPCI-6750 ordering information at the time of print. Contact your local Force Computers representative for current information.

Table 3 Excerpt from the Product's Ordering Information

Product name	**Description**
PPC/PowerCoreCPCI-6750/…	
...16-233-L512-4	PowerPC 750, 16-MByte EDO DRAM, 233-MHz nominal processor frequency, 512-KByte L2 cache, and 4-MByte user flash
...64-233-L512-4	PowerPC 750, 64-MByte EDO DRAM, 233-MHz nominal processor frequency, 512-KByte L2 cache, and 4-MByte user flash
...64S-300-L1024-8	PowerPC 750, 64-MByte SDRAM, 300-MHz nominal processor frequency, 1-MByte L2 cache, and 8-MByte user flash
...128S-300-L1024-8	PowerPC 750, 128-MByte SDRAM, 300-MHz nominal processor frequency, 1-MByte L2 cache, and 8-MByte user flash
...64S-400-L1024-8	PowerPC 750, 64-MByte SDRAM, 400-MHz nominal processor frequency, 1-MByte L2 cache, and 8-MByte user flash

Table 3 Excerpt from the Product's Ordering Information (cont.)

Product name	Description
...128S-400-L1024-8	PowerPC 750, 128-MByte SDRAM, 400-MHz nominal processor frequency, 1-MByte L2 cache, and 8-MByte user flash
PPC/PowerCore-…	
...MEM/128U	User upgradable upper EDO DRAM memory module, 128 MByte
...SMEM/128U	User upgradable upper SDRAM memory module, 128 MByte
Accessories	
ACC/IOBP/RTB860-E1-120	rear transition board to be used in conjunction with the PMC/860/xx-E1-R module where xx is the processor frequency in MHz
ACC/IOBP/RTB860-T1-100	rear transition board to be used in conjunction with the PMC/860/xx-T1-R module where xx is the processor frequency in MHz

3 Installation

This chapter provides important information for the installation of the PPC/PowerCoreCPCI-6750.
Before installing the PPC/PowerCoreCPCI-6750, read section “Safety Notes” on page xiii.

3.1 Installation Prerequisites and Requirements

Note: **Before powering up or plugging the board in, check this section for installation prerequisites and requirements and check the consistency of the current switch setting (see section 3.4 “Switch Settings” on page 17).**

3.1.1 Requirements

The installation requires only

- a power supply for 5 V and 3.3 V,
- a fan unit providing an airflow meeting the thermal requirements of the PPC/PowerCoreCPCI-6750,
- and a CompactPCI backplane with P1 and P2 connectors.

Power Requirements

The PPC/PowerCoreCPCI-6750 provides a limited current at the PMC supply pins. The maximum current depends on:

- the CPU type and frequency
- and the installed memory modules.

Typical power requirements of the board are given in the following table:

Table 1 Typical Power Requirements of the Board incl. Memory Module

Board with lower memory module but without PMC module	+5 V	3.3 V
PPC/PowerCoreCPCI-6750/16-233-L512-4	1.9 A	1.8 A
PPC/PowerCoreCPCI-6750/64-233-L512-4	2.2 A	1.9 A
PPC/PowerCoreCPCI-6750/64S-300-L1024-8	1.2 A	2.2 A
PPC/PowerCoreCPCI-6750/128S-300-L1024-8	1.2 A	2.2 A
PPC/PowerCoreCPCI-6750/64S-400-L1024-8	1.4 A	1.9 A
PPC/PowerCoreCPCI-6750/128S-400-L1024-8	1.4 A	1.9 A

Memory Modules

Per default the shared memory of the board is provided by one (lower) memory module directly located on the board. The following 2 types of memory modules are available:

- EDO DRAM memory module
- and SDRAM memory module.

If your board is equipped with one of the following lower memory modules, you may increase the capacity of the memory by installing an additional appropriate (upper) memory module on top of the lower one:

- 64-MByte EDO DRAM memory module
- 64- or 128-MByte SDRAM memory module.

All other memory modules per default installed on the board, for example the 16-MByte EDO DRAM memory module, cannot be upgraded.

Caution

When installing or uninstalling a memory module, observe the following safety notes:
The PPC/PowerCoreCPCI-6750 may be equipped only with memory modules qualified by Force Computers. Otherwise the board or connected components may be damaged.
Before installing or uninstalling the memory module turn off the power, since the memory modules do not provide hot-swap functionality.
Do not place an EDO DRAM memory module on top of an SDRAM memory module or vice versa.

Out of the comprehensive list of possible configurations the memory configurations shown in the following table have been qualified.

Table 2 Qualified Memory Module configurations

	PPC/PowerCore-…	
	MEM/128U	SMEM/128U
PPC/PowerCoreCPCI-6750/64-…	x	–
PPC/PowerCoreCPCI-6750/64S-…	–	x
PPC/PowerCoreCPCI-6750/128S-…	–	x

The upgrading instructions are shipped together with the memory modules: see the respective *Memory Module Installation Guide.*

When installing an upper memory module on the lower memory module installed per default on the board, you have to consider the power consumption. In this case add

- the power consumption of the board including lower memory module (see table 1 “Typical Power Requirements of the Board incl. Memory Module” on page 10)
- and the max. power consumption drawn by the upper memory module (see table 3 “Max. Power Consumption of the Upper Memory Modules”).

Table 3 Max. Power Consumption of the Upper Memory Modules

PPC/PowerCore-…	3.3 V
MEM/128U	0.1 A
SMEM/128U	0.2 A

PMC

The PPC/PowerCoreCPCI-6750 provides 2 PMC slots which can be used to install PMC modules based on the PCI bus architecture. The maximum permissible power consumption of each PMC module is 7.5 W.

Danger

Before installing or uninstalling a PMC module turn off the power, since the PMC modules do not provide hot-swap functionality.

Environmental Requirements

The following table summarizes the environmental requirements of the PPC/PowerCoreCPCI-6750.

Table 4 Environmental Requirements of the PPC/PowerCoreCPCI-6750

	Operating	**Non-operating**
Temperature	0°C to +55°C	–40°C to +85°C
Forced airflow	300 LFM (linear feet per minute)	–
Temp. change	+/– 0.5°C/min	+/– 1°C/min
Rel. humidity	5% to 95% noncondensing at +40°C	5% to 95% noncondensing at +40°C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m

The environmental conditions must be tested and proven in the used system configuration. These conditions refer to the surroundings of the board within the user environment. Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature. To meet the operating conditions, forced airflow is required at the heat sink of the CPU and at the top side of the board.

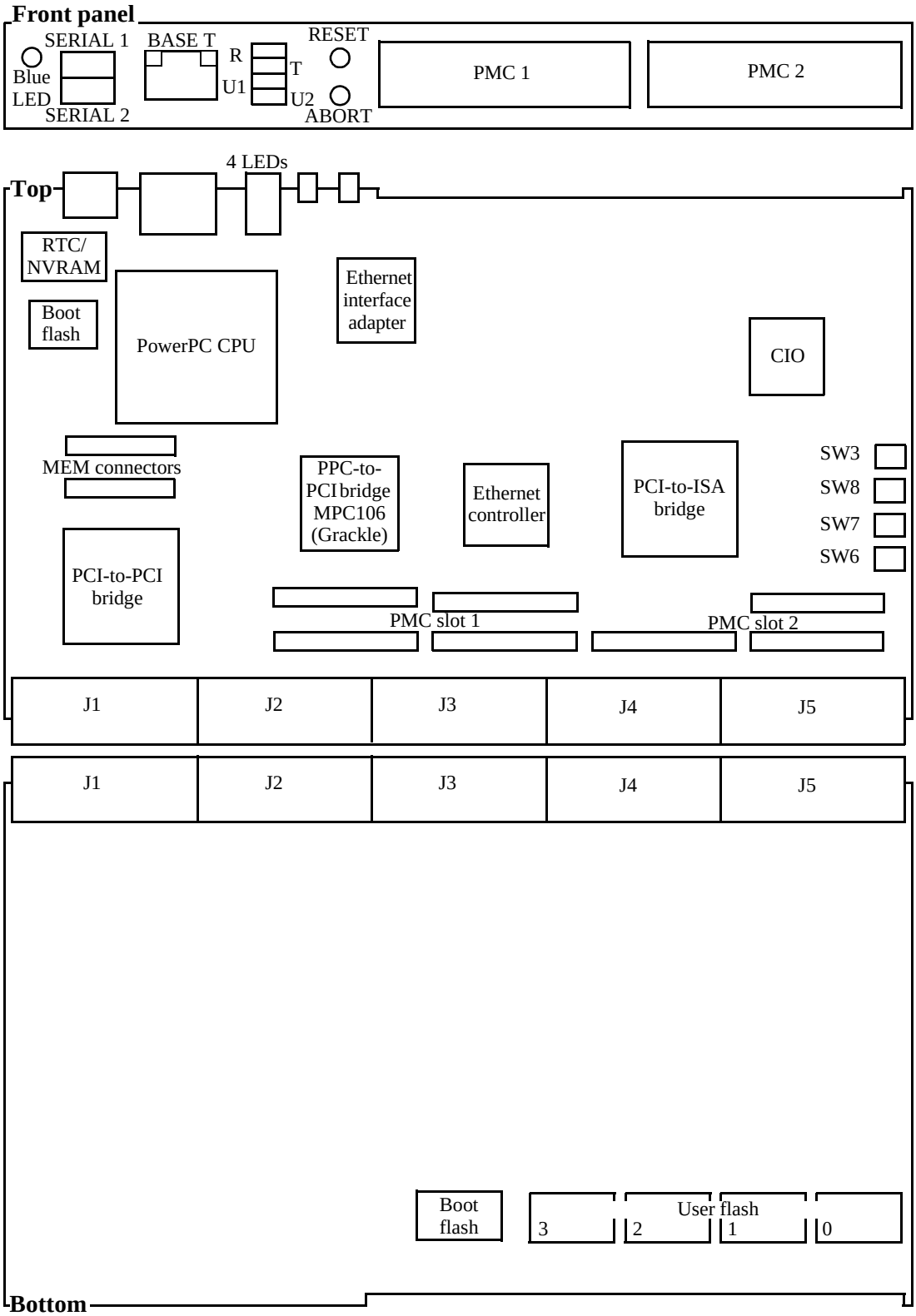
3.1.2 Terminal Connection

For the initial power-up, a terminal can be connected to the left 9-pin MicroD-Sub connector, which is located at the front panel (see section 3.7 “Serial I/O Ports” on page 20).

3.1.3 Location Overview

The figure 1 “Location diagram of the PPC/PowerCoreCPCI-6750 (schematic)” on page 13 shows the location of the important PPC/PowerCoreCPCI-6750 components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 1 Location diagram of the PPC/PowerCoreCPCI-6750 (schematic)



3.1.4 Upgrading the PPC/PowerCoreCPCI-6750

Memory Module

Depending on the (lower) memory module which is per default installed on the PPC/PowerCoreCPCI-6750, it is possible to increase the memory capacity of the board by installing an upper memory module on top of the (lower) memory module.
For detailed information on the memory modules, see

- section 3.1 “Installation Prerequisites and Requirements” on page 9
- and the respective *Memory Module Installation Guide*.

PMC Module

The PPC/PowerCoreCPCI-6750 provides 2 PMC slots. The PMC slots can be used to install PMC modules based on the PCI bus architecture.
For detailed information on the PMC modules, see

- section 3.1 “Installation Prerequisites and Requirements” on page 9
- and section 3.12 “PMC Slots” on page 25.

3.2 Installing Under Hot-Swap Conditions

The PPC/PowerCoreCPCI-6750 is a full hot-swap board. This covers board support in the following situations:

- The basic purpose of hot-swap support is to allow the board to be installed and uninstalled in a powered system without adversely affecting system operation. This is done for repairing faulty boards or reconfiguring a system.
- Additionally, hot-swap support provides programmatic access to hot-swap services allowing system reconfiguration and fault recovery to take place without system down time and with minimum operator interaction.
- Finally, hot-swap support allows the system to isolate faulty boards so that a system can continue operating in case of failure – possibly with reduced capability. This is especially useful in the area of high-availability applications, although typically other features may be in a prominent role to the user of high-availability applications.

The PPC/PowerCoreCPCI-6750 can be used in non hot-swap systems, basic hot-swap systems, full hot-swap systems, and high-availability systems. The PPC/PowerCoreCPCI-6750 provides the signals ENUM# and HEALTHY# for host or hot-swap-controller (HSC) notification, 4 control and status bits concerning hot-swap conditions, a hot-swap switch (integrated in the lower handle), and a blue LED to interface with the operator.

- After installing or before uninstalling the PPC/PowerCoreCPCI-6750 in a powered system, the interrupt ENUM# is generated and passed to the system board of the CompactPCI system to indicate a service request.
- A set of 4 control and status bits on each board allows the host software to determine the source of the ENUM# signal and control the hot-swap LED.
- The hot-swap switch allows the operator to indicate the intention to uninstall the board. The PPC/PowerCoreCPCI-6750 implements the hot-swap switch in the lower handle of the front panel.
- The blue hot-swap LED indicates that it is allowed to uninstall the board.

Note: **If hot-swap is supported by the system, at least the system documentation includes installation guidelines how to install or uninstall boards under hot-swap conditions. The system documentation includes both the hardware documentation and the software documentation. The hardware documentation covers chassis and installed boards – in CompactPCI hot-swap terms the platform. The software documentation covers the operating system, possibly additional drivers, and applications – in CompactPCI hot-swap terms all which makes a platform a system. Therefore: Refer to the documentation of all installed boards and to the system documentation. Never install or uninstall the PPC/PowerCoreCPCI-6750 in a system under hot-swap conditions unless the system documentation explicitly includes appropriate guidelines for these 2 tasks.**

Installing and Uninstalling

1. Start uninstalling the board by checking all installed boards for steps that you have to take before removing a board from a powered system.
2. Take those steps.
3. Open the lower front-panel handle to indicate removal.
4. Wait until the hot-swap LED turns blue.

Note: **As long as the hot-swap LED is off, the board is in normal operation and must not be removed.**

---

5. Remove the board from the powered system.
6. Reconfigure the board according to your needs or replace it by another board.

7. Start installing the reconfigured board or the replacement board by checking all boards for steps that you have to take before installing a board under hot-swap conditions:
   – Check the boards which are installed from the front side of the backplane.
   – Check the installation configuration of the rear I/O for the slot in which the board is going to be plugged in.
8. Take those steps.
9. Finally insert the board into the powered system.

   The hot-swap LED stays blue until the board hardware connection process has been completed.

3.3 Automatic Power Up – Voltage Sensor and Watchdog Timer

Voltage Sensors

If the 3.3-V or 5-V voltage level drops below the voltage values given in the CompactPCI specification, the voltage sensors generate automatically a reset of the board and proceed with a normal booting procedure. The +12-V and –12-V voltage levels are neither observed nor used by the PPC/PowerCoreCPCI-6750. If a PMC module uses the +12-V or –12-V voltage, the voltage must be observed by the PMC module.

Watchdog Timers

There are 2 watchdog timers available:

- watchdog timer 1
- and watchdog timer 2.

Per default both watchdog timers are disabled.

Watchdog Timer 1

Watchdog timer 1 can be enabled via SW8-1 (see table 5 “Default Switch Settings” on page 17). The expiry time can be selected via SW8-3 (see table 5 “Default Switch Settings” on page 17). If watchdog timer 1 is enabled, it generates a reset after the selected time has been expired.

Watchdog Timer 2

Watchdog timer 2 can be enabled via SW8-2 (see table 5 “Default Switch Settings” on page 17). The expiry time can be selected via SW8-3 (see table 5 “Default Switch Settings” on page 17). Depending on the setting of SW8-4 the enabled watchdog timer 2 generates

- a non-maskable interrupt (NMI)
- or a high-level interrupt

after the selected time has expired.

3.4 Switch Settings

The following table lists the functions and the default settings of all switches shown in figure 1 “Location diagram of the PPC/PowerCoreCPCI-6750 (schematic)” on page 13. The switches are located on the top side of the board. For switching it is not required to remove any modules.

Note: **Before powering up the board check the current switch settings for consistency.**

Note: **Do not switch during operation.**

Table 5 Default Switch Settings

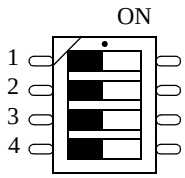
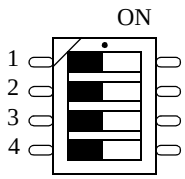
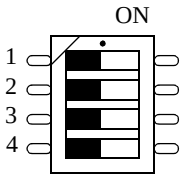
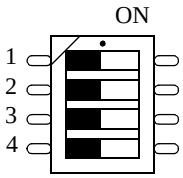
Name and default setting		Description
	SW3-1 OFF	If the signal FAL# is active, OFF = no interrupt is generated. ON = interrupt is generated.
	SW3-2 OFF	If the signal DEG# is active, OFF = no interrupt is generated. ON = interrupt is generated.
	SW3-3 OFF	reserved
	SW3-4 OFF	reserved
	SW6-1 OFF	Boot device selection OFF = Booting from PLCC device ON = Booting from TSOP device
	SW6-2 OFF	Boot flash write protection OFF = write-protected ON = writing enabled
	SW6-3 OFF	User flash write protection OFF = writing enabled ON = write-protected
	SW6-4 OFF	reserved

Table 5 Default Switch Settings (cont.)

Name and default setting		Description
	SW7-1 OFF	RESET key OFF = enabled ON = disabled
	SW7-2 OFF	ABORT key OFF = enabled ON = disabled
	SW7-3 OFF	reserved
	SW7-4 OFF	reserved
	SW8-1 OFF	Watchdog timer 1 OFF = disabled ON = enabled
	SW8-2 OFF	Watchdog timer 2 OFF = disabled ON = enabled
	SW8-3 OFF	Watchdog time OFF = NMI: ~32 ms, RESET: ~0.5 s ON = NMI: ~500 ms, RESET: ~2.5 s
	SW8-4 OFF	If SW8-2 is ON, watchdog timer 2 generates OFF = NMI ON = high-level interrupt

3.5 Front Panel

The features of the front panel are described in the following table. For a location diagram see figure 1 “Location diagram of the PPC/PowerCoreCPCI-6750 (schematic)” on page 13.

Table 6 Front-panel Features

Device	Description
RESET	Mechanical reset key: When enabled and toggled it instantaneously affects the board by generating a reset. A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. To avoid unintentional reset, the reset key is recessed in the front panel. For information on enabling the key see “SW7-1” on page 18.
ABORT	Mechanical abort key: When enabled and toggled it instantaneously affects the board by generating a non-maskable interrupt (NMI) request via the PCI-to-ISA bridge. This allows to implement an abort of the current program, to trigger a self-test, or to start a maintenance program. To avoid unintentional abort, the abort key is recessed in the front panel. For information on enabling the key see “SW7-2” on page 18.
LED R	RUN/RESET LED indicating the board status: • green: normal operation • red: reset is active
LED T	Test LED: For factory test. Off during normal operation.
LED U 1	User LED 1: Software programmable by the CIO counter/timer and parallel I/O unit. Bits 0 and 1 of port C are used. Possible status: green, red, or off.
LED U 2	User LED 2: Software programmable by the CIO counter/timer and parallel I/O unit. Bits 2 and 3 of port C are used. Possible status: green, red, or off.
100Base-Tx 10Base-T ETHERNET	An 8-pin RJ-45 connector for the interfaces 100Base-Tx or 10Base-T Ethernet including 2 LEDs: • The green LED stays lit while the Ethernet is linked. • The yellow LED lits when collisions on the Ethernet are detected.
SERIAL PORTS	A double 9-pin MicroD-Sub connector for 2 serial ports (see section 3.7 “Serial I/O Ports” on page 20).
Hot-swap LED	Blue hot-swap LED: • blue: board is plugged in or may be removed from the system • off: board must not be removed from the system
Hot-swap switch	Hot-swap switch integrated in the lower handle. When the handle is opened during normal operation the interrupt signal ENUM# is asserted on the CompactPCI backplane. This interrupt indicates insertion of a new board or the pending removal of a board.

3.6 PPC/PowerCoreCPCI-6750 Parameters and Timers – CIO

Device: CIO	
Frequency	4.125 MHz
Accessible from	PowerPC processor
Access base address	ISA: 0000.0300_{16} PCI: 0000.0300_{16} CPU: $FE00.0300_{16}$
Port width	8 bit
Interrupt request	Priority level 8 (software reprogrammable, IRQ13)

Configurable Parameters

Via the CIO device several parameters can be configured or read respectively: user flash device select, user flash page select, boot flash page select (if boot flash has a capacity of 1 MByte or more), watchdog trigger, user LED control, ID-ROM (serial EEPROM), PCI busmode signals, and the three 16-bit timers.

Timers

Three 16-bit timers with a resolution of approximately 500 ns are available.

3.7 Serial I/O Ports

The PPC/PowerCoreCPCI-6750 provides 2 serial I/O ports:

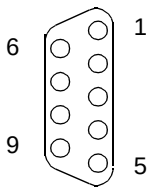
- serial I/O port 1
- and serial I/O port 2.

	Serial I/O port 1	**Serial I/O port 2**
Frequency	1.8432 MHz	
Accessible from	PowerPC processor	
Access base address	ISA: $0000.03F8_{16}$ PCI: $0000.03F8_{16}$ CPU: $FE00.03F8_{16}$	ISA: $0000.02F8_{16}$ PCI: $0000.02F8_{16}$ CPU: $FE00.02F8_{16}$
Port width	8 bit	
Interrupt request	Priority level 12 (software reprogrammable, IRQ4)	Priority level 11 (software reprogrammable, IRQ3)

Connector Availability

The RS-232 serial I/O ports 1 and 2 are each available via a double 9-pin MicroD-Sub connector at the front panel.

Table 7 Pinout of the Front-Panel Serial I/O Ports for RS-232



Pin	Signal
1	DCD (Data Carrier Detect, input)
2	RXD (Receive Data, input)
3	TXD (Transmit Data, output)
4	DTR (Data Terminal Ready, output)
5	GND (Ground)
6	DSR (Data Set Ready, input)
7	RTS (Request to Send, output)
8	CTS (Clear to Send, input)
9	GND (Ground)

Port Setup

- RS-232 asynchronous communication
- 9600 baud, 8 data bits, 1 start bit, 1 stop bit, no parity
- no handshake protocol used per default

3.8 PCI-to-ISA Interface

Device: PCI-to-ISA bridge	
Frequency	PCI bus frequency of 33 MHz
Accessible from	PowerPC processor
IDSEL	AD30
Access base address	not defined
Port width	32 bit
Interrupt request	not defined

The PCI bus interface is 32-bit wide and able to transfer data via the internal DMA controller.

The PCI-to-ISA bridge provides a high-performance interface between PCI bus and ISA bus. This interface is capable of accelerating PIO data transfers and to act as PCI bus master on behalf of an IDE DMA slave device. First, the slave device declares that it wants to be served by the PCI-to-ISA bridge master by requesting DMA.

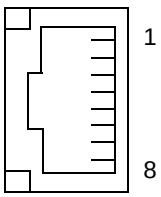
3.9 Ethernet Interface

Device: Ethernet controller	
Frequency	PCI bus frequency: 33 MHz
Accessible from	PowerPC processor
IDSEL	AD25
Access base address	PCI: 0080.0000_{16} CPU: $FE85.0000_{16}$
Port width	32 bit
Interrupt request	Priority level 4 (INTA#, IRQ9)

The Ethernet interface 10Base-T or 100Base-TX is available at the front panel via an 8-pin RJ-45 connector. The PCI bus interface is 32-bit wide and able to transfer data via the on-chip DMA with programmable PCI burst size. The following table shows the pinout of the factory default Ethernet connector.

Table 8 8-pin RJ-45 Connector

8-pin RJ-45



Pin	Signal
1	TXP
2	TXM
3	RXP
4	n.c.
5	n.c.
6	RXM
7	n.c.
8	n.c.

3.10 CompactPCI Interface

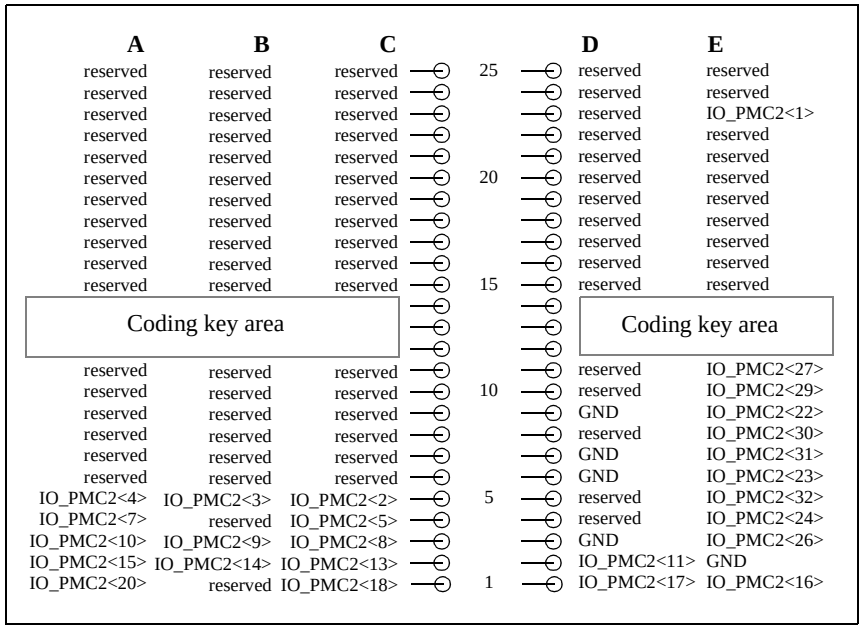
Device: PCI-to-PCI bridge	
Frequency	PCI bus frequency: 33 MHz
Accessible from	PowerPC processor
IDSEL	AD24
Access base address	PCI: 0086.0000_{16} CPU: $FE86.0000_{16}$
Port width	32 bit
Interrupt request	Priority level 3 (INTA#, IRQ9)

The PCI-to-PCI bridge provides a high-performance interface between the local PCI bus and the CompactPCI bus. The primary side of the PCI-to-PCI bridge is connected to the CompactPCI bus, the secondary side of the PCI-to-PCI bridge is connected to the local PCI bus. Both buses are 32-bit wide and run with up to 33 MHz.
The CompactPCI interface is a peripheral interface and can be used in a hot-swap system environment.

3.11 CompactPCI Connector Pinout

The following 2 figures show the user I/O signals available on the CompactPCI connectors J4 and J5. The signals named IO_PMC1<*x*> and IO_PMC2<*x*> are the user defined I/O signals from the PMC I/O connectors of the PMC modules 1 and 2, respectively, where *x* corresponds to the pin number of the PMC I/O connector.

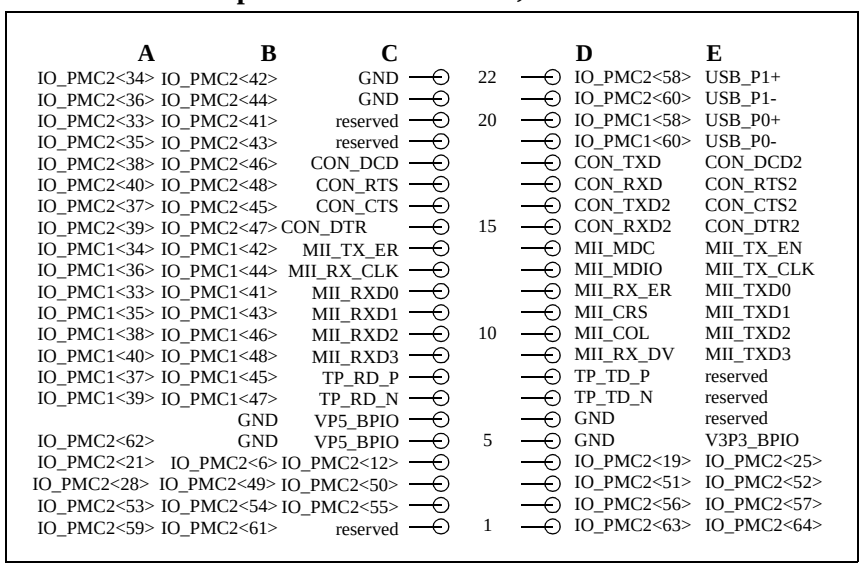
Figure 2 **Pinout of the CompactPCI Connector J4, Rows A…E**



Caution

Note that the reserved pins must not be connected.

Figure 3 **Pinout of the CompactPCI Connector J5, Rows A…E**



Caution

Note that the reserved pins must not be connected.

3.12 PMC Slots

The PPC/PowerCoreCPCI-6750 provides 2 PMC slots for installing PMC modules compliant with the *IEEE P1386.1/Draft 2.0 - Layers for PCI Mezzanine Cards: PMC* specification. The PCI bus, a high-speed local bus, connects different high-speed I/O cards with the PPC/PowerCoreCPCI-6750. Both PMC slots support 32-bit data bus width with a frequency of 33 MHz.

Power of the PMC Modules

For information on the power and requirements of the PMC modules, see section 3.1 “Installation Prerequisites and Requirements” on page 9.

3.12.1 PMC Voltage Keys

The PCI bus uses a 5-V voltage to signal bus levels. The voltage keys prevent 3.3-V PMC cards from being plugged into the PMC slots.

3.12.2 Connector Configuration

The 32-bit PCI bus requires 2 PMC connectors. The 3rd PMC connector connects additional user I/O signals of the PMC slots 1 and 2 with the CompactPCI bus J4 and J5 connectors.

PMC Slot 1 Connectors

- PN11 and PN12: for the PCI bus
- PN14: for 64 user I/O signals

PMC Slot 2 Connectors

- PN21 and PN22: for the PCI bus
- PN24: for 64 user I/O signals

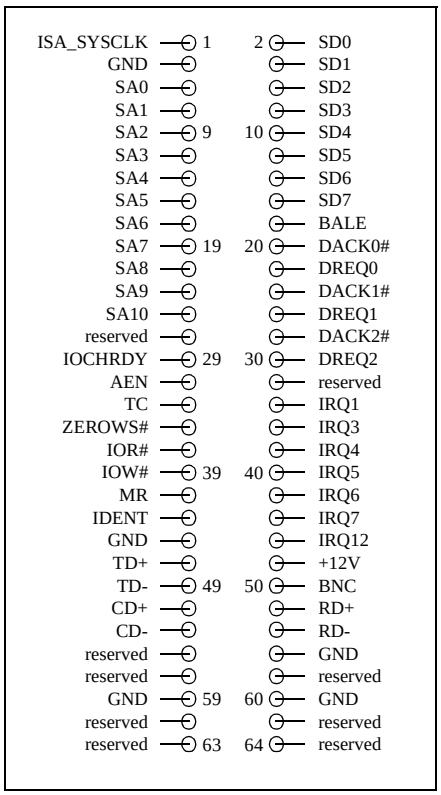
Caution

PMC slot 1 and PMC slot 2 have each 64 user I/O signals. All signals of the PMC slot 2 are available on the connectors J4 and J5. The I/O signals of the PMC slot 1 are partially available on the J5 connector (see figure 2 “Pinout of the CompactPCI Connector J4, Rows A…E” on page 24 and figure 3 “Pinout of the CompactPCI Connector J5, Rows A…E” on page 24).

3.12.3 ISA Connector

The connector PN15 is a factory option and makes a set of ISA bus signals available including 7 AUI signals.
The following figure shows the signals available on the ISA connector.

Figure 4 PN15 Connector Pinout



Caution

Note that the reserved pins must not be connected.

3.13 Testing the Board Using PowerBoot

PowerBoot is firmware providing some basic test and debug commands. It is stored in the on-board boot PROM.

Booting Up PowerBoot

PowerBoot automatically starts during power up or reset. After the successful pass of the self-initialization routine, the following message or a similar one will appear on the screen:

```
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller at address: 0xFE850000
Found PCI-to-PCI bridge at address: 0xFE860000
Found CPU740/750, PVR=00080202,
CPU clock: 251MHz, Bus clock: 83MHz, 8
DRAM EDO mode enab
, DRAM ECC mode enabled
Onboard DRAM      : none
Init DRAM Module 1:  16MB, 0x00000000..0x00FFFFFF
Init DRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 125MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board
Ethernet: 00:80:42:0E:1A:2E
Read DEC SROM...done - CRC is OK
PMC1/2: no auto mapping setup

<<PowerBoot V2.04 for PowerCore CPCI CPU-67X0>>

PowerBoot>
```

Starting a Test after Booting

To test the board for correct operation enter `probepci. probepci` does not provide a full-featured power-on self-test. However, it tests

some I/O devices and scans the PCI bus for participants. Depending on the board configuration, the following message will appear:

```
PowerBoot> probepci
Probing PCIbus at 0x80000000
Device ID = 0x0002; Vendor ID = 0x1057;
Status    = 0x0080; Command   = 0x0146;
Base Class= 0x06;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x40;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x00000000, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x00;   IRQ Line = 0x00;
Found PCI device: Motorola MPC106 PowerPC PCI bridge

Probing PCIbus at 0x8000C000
Device ID = 0x0046; Vendor ID = 0x1011;
Status    = 0x0290; Command   = 0x0007;
Base Class= 0x06;   Sub Class = 0x80;   Prg. Inter= 0x00;   Rev. ID   = 0x00;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x00;
base addr0= 0xFFFFF000, base addr1= 0x00860001;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x01;   IRQ Line = 0x00;
Found PCI device: DEC 21554 PCI-to-PCI Bridge

Probing PCIbus at 0x8000C800
Device ID = 0x0019; Vendor ID = 0x1011;
Status    = 0x0280; Command   = 0x0005;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x30;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x00;
base addr0= 0x00850001, base addr1= 0xFFFFFF80;
Max Lat   = 0x28;   Min Gnt   = 0x14;   IRQ Pin   = 0x01;   IRQ Line = 0x40;
Found PCI device: DEC 21143 PCI/Cardbus Ethernet LAN

Probing PCIbus at 0x8000F000
Device ID = 0x0565; Vendor ID = 0x10AD;
Status    = 0x0200; Command   = 0x0007;
Base Class= 0x06;   Sub Class = 0x01;   Prg. Inter= 0x00;   Rev. ID   = 0x10;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x00;
base addr0= 0x00000000, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x00;   IRQ Line = 0x00;
Found PCI device: Winbond W83C553F Sys. I/O Con., function 0

Probing PCIbus at 0x8000F100
Device ID = 0x0105; Vendor ID = 0x10AD;
Status    = 0x0280; Command   = 0x0000;
Base Class= 0x01;   Sub Class = 0x01;   Prg. Inter= 0x8F;   Rev. ID   = 0x05;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x000001F1, base addr1= 0x000003F5;
Max Lat   = 0x28;   Min Gnt   = 0x02;   IRQ Pin   = 0x01;   IRQ Line = 0x0E;
Found PCI device: Winbond W83C553F IDE, function 1

Probing PCIbus at 0x8000F800
PowerBoot>
```

3 Hardware

The PPC/PowerCoreCPCI-6750 is a high-performance single-slot PowerPC based platform providing a 32-bit CompactPCI bus interface. The CompactPCI bus interface device is directly connected to the local PCI bus. The board is based on:

- the PowerPC CPU (see section 3.4 “PowerPC CPU” on page 39),
- and on the CompactPCI bus (see section 3.11 “PCI-to-PCI Bridge” on page 58).

Described Features

The PPC/PowerCoreCPCI-6750 provides

- shared memory implemented via a memory module (see section 3.6 “Shared Memory” on page 41)
- boot flash (see section 3.7 “Boot Flash” on page 47)
- user flash (see section 3.8 “User Flash” on page 50)
- watchdog timers (see section 3.9 “Watchdog Timers” on page 53)
- a peripheral CompactPCI bus interface (see section 3.11 “PCI-to-PCI Bridge” on page 58)
- an Ethernet interface available via the front panel (see section 3.12 “Ethernet Interface” on page 60)
- an on-board real-time clock with on-board battery backup (see section 3.14 “Real-Time Clock / Non-Volatile RAM” on page 65)
- 2 RS-232 compatible serial I/O ports (see section 3.17 “Serial I/O Ports – SCCs” on page 73)
- 2 PMC slots with user I/Os available at the CompactPCI connectors J4 and J5 (see section 3.18 “PMC Slots” on page 74)

DMA Controllers

The following devices are collectively referred to as DMA controllers of the PPC/PowerCoreCPCI-6750 because they themselves provide an on-chip DMA controller:

- PCI-to-ISA bridge
- Ethernet controller

Front-Panel Interfaces

The front panel of the PPC/PowerCoreCPCI-6750 provides

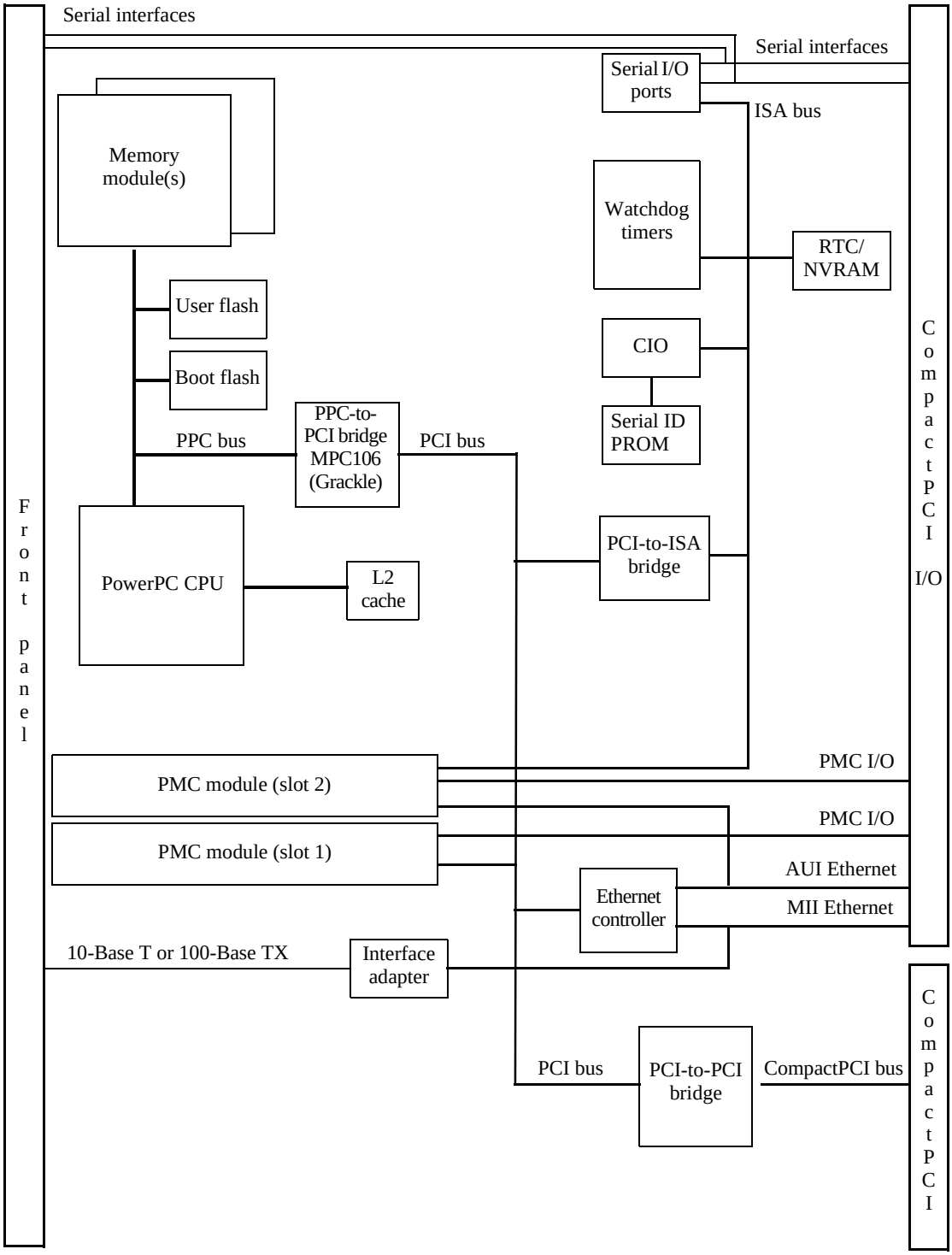
- an Ethernet interface for 10Base-T or 100Base-Tx (see section 3.12 “Ethernet Interface” on page 60)
- and 2 serial I/O ports (see section 3.17 “Serial I/O Ports – SCCs” on page 73). These ports serve as console port, for download and for data communication.

Factory Options

The following factory options are available:

- type and capacity of shared memory (see section 3.6 “Shared Memory” on page 41)
- processor clock frequency (see section 3.4 “PowerPC CPU” on page 39)
- capacity of user flash (see section 3.8 “User Flash” on page 50)
- capacity of L2 cache (see section 3.5 “L2 Cache” on page 40)
- PN15 connector (see section 2.12.3 “ISA Connector” on page 22)

Figure 5 PPC/PowerCoreCPCI-6750 Block Diagram



Bus overview

The following table gives an overview of the different buses, their busmodes, and the connected devices.

Table 12 Buses, Busmodes, and Connected Devices

Bus	Busmode	Connected devices
PPC bus	Big endian mode	PowerPC CPU Shared memory Boot flash User flash PPC-to-PCI bridge
PCI bus	Little endian mode	Ethernet controller PMC slots 1 and 2 PCI-to-PCI bridge PPC-to-PCI bridge PCI-to-ISA bridge
CompactPCI bus	Little endian mode	CompactPCI connectors J1 and J2 PCI-to-PCI bridge
ISA bus	Little endian mode	CIO RTC/NVRAM Serial I/O ports 1 and 2 DRAM and cache configuration register (DCCR) Board status and capability registers (BSCRs) PCI-to-ISA bridge

Bus frequencies

The bus frequencies depend on the CPU type and its frequency. The following table shows the frequencies of the different buses:

Table 13 Bus Frequencies

	Bus frequency [MHz]		
CPU type and frequency	**ISA**	**PCI**	**PPC**
PowerPC 750/233	8.25	33	66
PowerPC 750/300	8.25	33	82.5
PowerPC 750/400	8.25	33	82.5

3.1 PPC/PowerCoreCPCI-6750 Address Map

The PPC/PowerCoreCPCI-6750 provides a CHRP compliant address map. The following tables show the address maps of the PPC/PowerCoreCPCI-6750:

- PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU (addresses on the processor bus),
- PPC/PowerCoreCPCI-6750 Memory Map seen from the PCI (memory space addresses on the PCI bus),
- PPC/PowerCoreCPCI-6750 I/O Map seen from the PCI (I/O space addresses on the PCI bus),
- PPC/PowerCoreCPCI-6750Configuration Base Addresses (configuration addresses for the on-board PCI devices),
- PPC/PowerCoreCPCI-6750 ISA Bus Ports seen from the CPU (physical addresses for the on-board ISA devices),
- PPC/PowerCoreCPCI-6750 PCI I/O Devices seen from the CPU (physical addresses for the on-board PCI I/O devices).

IMPORTANT

- Before erasing or programming the boot flash ensure that you do not destroy the Force Computers PowerBoot boot image and make a copy of the boot flash device in socket J36 by using a programmer.
- Always remember the following access rule for any reserved bits in any PPC/PowerCoreCPCI-6750 register: written as `0`, read as undefined.
- All registers must be written or read using the data path width documented for the respective register.

Table 14 PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU

Address on the PPC bus	Device	Accessible bus		Cache		Bus width [bit]
		PCI	Compact PCI	L1	L2	
0000.0000_{16} … $3FFF.FFFF_{16}$	Shared memory space consisting of: • lower memory module • (and upper memory module) The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
4000.0000_{16} … $7FFF.FFFF_{16}$	reserved	–	–	–	–	–
8000.0000_{16} … $FCFF.FFFF_{16}$	PCI memory space CompactPCI memory space	Y	Y	N	N	[32]
$FD00.0000_{16}$ … $FDFF.FFFF_{16}$	PCI/ISA memory space 0000.0000_{16} … $00FF.FFFF_{16}$ on PCI (see table 16 “PPC/PowerCoreCPCI-6750 I/O Map seen from the PCI” on page 32)	Y	Y	N	N	[8]
$FE00.0000_{16}$ … $FE7F.FFFF_{16}$	ISA bus ports (see table 18 “PPC/PowerCoreCPCI-6750 ISA Bus Ports seen from the CPU” on page 33)	Y	Y	N	N	[8]
$FE80.0000_{16}$ … $FEBF.FFFF_{16}$	PCI I/O space 0080.0000_{16} … $00BF.FFFF_{16}$ on PCI (see table 16 “PPC/PowerCoreCPCI-6750 I/O Map seen from the PCI” on page 32)	Y	Y	N	N	[32]
$FEC0.0000_{16}$ … $FEDF.FFFF_{16}$	Configuration address register of the PPC-to-PCI bridge	Y	Y	N	N	[32]
$FEE0.0000_{16}$ … $FEEF.FFFF_{16}$	Configuration data register of the PPC-to-PCI bridge	N	N	N	N	[32]
$FEF0.0000_{16}$ … $FEFF.FFFF_{16}$	PCI interrupt acknowledge	N	N	N	N	[32]
$FF00.0000_{16}$ … $FFDF.FFFF_{16}$	reserved	–	–	–	–	–

Table 14 PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU (cont.)

Address on the PPC bus	Device	Accessible bus		Cache		Bus width [bit]
		PCI	Compact PCI	L1	L2	
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash space	Y	Y	Y	Y	[8]
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	Boot flash space	Y	Y	Y	Y	[8]

Table 15 PPC/PowerCoreCPCI-6750 Memory Map seen from the PCI

PCI memory address	Device	Accessible bus		Cache		Bus width [bit]
		PPC	Compact PCI	L1	L2	
0000.0000_{16} … $3FFF.FFFF_{16}$	Shared memory space consisting of: • lower memory module • (and upper memory module) The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
4000.0000_{16} … $7FFF.FFFF_{16}$	reserved	–	–	–	–	–
8000.0000_{16} … $FCFF.FFFF_{16}$	PCI memory space CompactPCI memory space	Y	Y	N	N	[32]
$FD00.0000_{16}$ … $FDFF.FFFF_{16}$	Shared memory space 0000.0000_{16} ... $00FF.FFFF_{16}$ (see table 14 “PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU” on page 30)	Y	Y	N	N	[32]
$FE00.0000_{16}$ … $FFDF.FFFF_{16}$	reserved	–	–	–	–	–
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash space	Y	Y	Y	Y	[8]
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	Boot flash space	Y	Y	Y	Y	[8]

Table 16 PPC/PowerCoreCPCI-6750 I/O Map seen from the PCI

PCI I/O address	Device	Accessible bus		Cache		Bus width [bit]
		PPC	Compact PCI	L1	L2	
0000.0000_{16} … $0000.FFFF_{16}$	ISA I/O space $FE00.0000_{16}$ ... $FE00.FFFF_{16}$ on PowerPC CPU (see table 14 “PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU” on page 30)	Y	Y	N	N	[8]
0001.0000_{16} … $007F.FFFF_{16}$	reserved	–	–	–	–	–
0080.0000_{16} … $00BF.FFFF_{16}$	PCI I/O space $FE80.0000_{16}$ ... $FEBF.FFFF_{16}$ on PowerPC CPU (see table 14 “PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU” on page 30)	Y	Y	N	N	[32]
$00C0.0000_{16}$ … $FFFF.FFFF_{16}$	reserved	–	–	–	–	–

Table 17 PPC/PowerCoreCPCI-6750Configuration Base Addresses

Configuration base address	Device
8000.0000_{16}	Base address
$8000.C000_{16}$	PCI-to-PCI bridge
$8000.F000_{16}$	PCI-to-ISA bridge
$8000.F100_{16}$	PCI-to-ISA bridge (IDE function not supported)
$8000.C800_{16}$	Ethernet controller
$8000.D000_{16}$	PMC 1
$8000.D800_{16}$	PMC 2

Table 18 PPC/PowerCoreCPCI-6750 ISA Bus Ports seen from the CPU

Address	Device
$FE00.0073_{16}$	RTC/NVRAM address low register
$FE00.0074_{16}$	reserved
$FE00.0075_{16}$	RTC/NVRAM address high register
$FE00.0077_{16}$	RTC/NVRAM/RTC data register
$FE00.02F8_{16}$ … $FE00.02FF_{16}$	Serial I/O port 2
$FE00.0300_{16}$ … $FE00.0303_{16}$	CIO registers
$FE00.0308_{16}$	DRAM and cache configuration register (DCCR)
$FE00.0312_{16}$ … $FE00.0340_{16}$	Board status and capability registers (BSCRs). The addresses in this range which are not described in section 3.16 “Board Status and Capability Registers - BSCRs” on page 69 are reserved.
$FE00.03F8_{16}$ … $FE00.03FF_{16}$	Serial I/O port 1

Table 19 PPC/PowerCoreCPCI-6750 PCI I/O Devices seen from the CPU

Address	Device
$FE81.0000_{16}$ … $FE81.0FFF_{16}$	PCI-to-PCI bridge
$FE85.0000_{16}$ … $FE85.003F_{16}$	Ethernet controller
user defined	PMC 1
user defined	PMC 2
$FEC0.0000_{16}$ … $FEDF.FFFF_{16}$	PCI configuration address register
$FEE0.0000_{16}$ … $FEEF.FFFF_{16}$	PCI configuration data register
$FEF0.0000_{16}$ … $FEFF.FFFF_{16}$	PCI interrupt acknowledge register

IMPORTANT

This address map is a default address map which can be changed by the user.

3.2 PPC/PowerCoreCPCI-6750 Interrupt Map

The PCI-to-ISA bridge monitors all PPC/PowerCoreCPCI-6750 interrupt requests (IRQs):

Interrupt Requests

- interrupt requests of all 4 PCI bus interrupt levels
- interrupt requests from on-board ISA bus devices, e.g. from the serial controller
- optional interrupt requests (see figure 4 “PN15 Connector Pinout” on page 22)
- CompactPCI related interrupt requests (see SW3-1 and SW3-2 in table 8 “Default Switch Settings” on page 13)

PCI-to-ISA Bridge Interrupt Controller

The PCI-to-ISA bridge provides an ISA compatible interrupt controller that incorporates the functionality of 2 interrupt controllers. The 2 controllers are cascaded so that 13 chip external and 3 chip internal interrupts are possible.
For information on programming the interrupt controller, see section 3.13.2 “Interrupt Controller” on page 63.

Flexible Interrupt Programming

Every interrupt source can be enabled and disabled to interrupt the CPU. The PCI-to-ISA bridge supplies the interrupt vectors for all interrupts except the non-maskable interrupt (NMI).

NMI

The NMI is routed from the IOCHK interrupt via the PPC-to-PCI bridge to the MCP# signal at the PowerPC CPU. The NMI has the highest priority and is a non-vectored processor exception.

Interrupt Priority

The following table shows the default mapping of the interrupts and their interrupt priority. Interrupt priority level 0 is the highest priority, level 15 is the lowest priority. The mapping of the interrupts and the interrupt priority can be set also by the user.

Table 20 Default PPC/PowerCoreCPCI-6750 Interrupt Map

Function	Device	PCI-to-ISA bridge IRQ	Interrupt priority level
Watchdog timer/ abort key/SERR#	Dedicated logic	IOCHK (MCP#), NMI	0
Timer 1/counter 0	PCI-to-ISA bridge	IRQ0	1
User available	PN15 connector (factory option)	IRQ1	2
Cascade	PCI-to-ISA bridge	IRQ2	-
Serial port 2	Serial port 2	IRQ3	11
Serial port 1	Serial port 1	IRQ4	12
User available	PN15 connector (factory option)	IRQ5	13
User available	PN15 connector (factory option)	IRQ6	14
User available	PN15 connector (factory option)	IRQ7	15
Watchdog timer (optional routing)	Dedicated logic (see SW8-4 in table 8 “Default Switch Settings” on page 13)	IRQ8#	3
INTA#	PCI device: PCI-to-PCI bridge	IRQ9	4
INTB#	PCI device: Ethernet controller	IRQ10	5
INTC#	PCI devices	IRQ11	6
User available	PN15 connector (factory option)	IRQ12	7
Timer/parallel port IRQ	CIO	IRQ13	8
CompactPCI signals FAL# and DEG#	Dedicated logic (see SW3-1 and SW3-2 in table 8 “Default Switch Settings” on page 13)	IRQ14	9
INTD#	PCI devices	IRQ15	10

The following table shows the interrupt routing of the PMC slots.

Table 21 PMC Interrupt Routing

Interrupt lines		
PCI-to-ISA bridge	**PMC slot 1**	**PMC slot 2**
INTA#	INTC#	INTD#
INTB#	INTD#	INTA#
INTC#	INTA#	INTB#
INTD#	INTB#	INTC#

3.3 Hot-Swap Support

The PPC/PowerCoreCPCI-6750 supports full hot-swap systems and high-availability systems as defined by the *CompactPCI Hot Swap Specification PICMG 2.1 R1.0.*

The hot-swap capability of the PPC/PowerCoreCPCI-6750, which is a peripheral board, is based upon

- a power control logic to power the board if enabled by the system,
- a precharge circuitry,
- and a hot-swap control and status register informing the system board about the current hot-swap status and controlling the interface to the user.

When installing the PPC/PowerCoreCPCI-6750 into a hot-swap CompactPCI system, the following main processes may take place:

- connecting the board (physical connection process)
- controlling the board connection (hardware connection process)
- controlling the board connection via system software (software connection process)

Connecting the Board

To use the hot-swap features of the PPC/PowerCoreCPCI-6750, the CompactPCI system must provide pin staging as defined in the *CompactPCI Hot Swap Specification PICMG 2.1 R1.0* so that the different connection levels can be recognized. The board connection includes the following steps:

1. At first the longest pins (1st-level pins) are connected. They supply the on-board hot-swap logic to indicate the user via the blue hot-swap

LED that a hot-swap process takes place and to precharge the 2nd-level pins.

2. The 2nd-level pins are precharged in order to avoid PCI cycles running on the backplane from being disturbed during connecting the 2nd-level pins.
3. Finally, the 3rd-level pins are connected. They provide the board connection control signals, which may be appraised and controlled by a hot-swap controller.

Controlling the Board Connection

After the board has been connected the controlling of the connection takes place. The board connection control includes the following steps:

4. When the board connection has been finished and a logic low is detected on the CompactPCI signal BDSEL# provided by a 3rd-level pin, the supply voltages for the board are ramped up.
5. When all voltages have reached their appropriate values, the feedback signal HEALTHY# is driven to the CompactPCI interface.
6. HEALTHY# is used together with the CompactPCI reset signal (logical OR) to generate a separate reset signal for the PCI-to-PCI bridge, and thus for the PPC/PowerCoreCPCI-6750.
7. When the reset signal for the PCI-to-PCI bridge is inactive, the board connection control is finished. Now, after configuring the PCI-to-PCI bridge appropriately, accesses from a CompactPCI bus device to the PCI-to-PCI bridge are possible.

Controlling the Board Connection via Software

After the board connection control further operation will be controlled via software. The software connection control includes the following steps:

8. After the PPC/PowerCoreCPCI-6750 has been installed, it asserts the signal ENUM# to the CompactPCI backplane. This signal is used in a full hot-swap or high-availability environment to inform the CPU of the system board or a hot-swap-controller (HSC) that a hot-swap process takes place and that the system configuration is to be changed.
9. The system software reconfigures the hardware and sets or clears the hot-swap control and status register bits appropriately to control the further generation of ENUM# signals and the illumination of the blue hot-swap LED (see table 22 “Hot-swap Control and Status Register, Bits [7…6], [3], and [1]” on page 38).

Table 22 Hot-swap Control and Status Register, Bits [7…6], [3], and [1]

Bit	7	6	5	4	3	2	1	0
Value	INS_ STAT	REM_ STAT	reserved		L_STAT_ CNTL	reserved	ENUM_ MASK	reserved

IMPORTANT

The hot-swap control and status register is accessible in the PCI configuration space from both sides of the PCI-to-PCI bridge (CompactPCI and local PCI). The bridge is accessible from the local PCI bus number 00_{16}, device number 18_{16}, function number 00_{16}. The register number is $0000.00EE_{16}$. The register location from the CompactPCI bus is system specific and therefore beyond the scope of this manual.

INS_STAT (R/W)

INS_STAT indicates the status during the installation of the board.

= 0 no effect

= 1 ENUM# is asserted to the CompactPCI backplane to indicate that the board has just been inserted. After this INS_STAT will be cleared.

REM_STAT (R/W)

REM_STAT indicates the status during removing the board from the system.

= 0 no effect

= 1 ENUM# is asserted to the CompactPCI backplane to indicate that the board is about to be removed. After this REM_STAT will be cleared.

L_STAT_CNTL (R/W)

L_STAT_CNTL indicates the status of the blue hot-swap LED.

= 0 Hot-swap LED is on.

= 1 Hot-swap LED is off.

ENUM_MASK (R/W)

ENUM_MASK indicates whether the interrupt signal ENUM# is asserted on the CompactPCI backplane.

= 0 The ENUM# interrupt is asserted when the board is inserted or about to be removed.

= 1 The ENUM# interrupt is not asserted when the board is inserted or about to be removed.

Removing the Board

To remove the PPC/PowerCoreCPCI-6750 from the system

- open the front-panel handles; by this the interrupt signal ENUM# is asserted to the CompactPCI backplane to indicate a pending removal. This interrupt requests the board to be quiesced by system software if available.

- or quiesce the board and all processes via CompactPCI directly via software (basic hot swap).

Afterwards, the hot-swap control and status register bits are appropriately set so that the hot-swap LED turns blue. Now, the board may be physically disconnected from the system.

3.4 PowerPC CPU

The microprocessor PowerPC 750 is one of the basic components of the PPC/PowerCoreCPCI-6750.

For detailed information refer to the *PowerPC User's Manual* available from Motorola Semiconductors.

The PowerPC 750 consists of a processor core and an internal L2 tag RAM combined with a dedicated L2 cache interface and a PCI bus. It provides:

- 32-bit effective addresses,
- integer data types of 8, 16, and 32 bits,
- and floating-point data types of 32 and 64 bits.

Execution Units

The PowerPC 750 is a superscalar processor sustaining a peak throughput of 3 instructions per clock. It includes the following independent execution units:

- a control unit,
- a floating-point unit,
- 2 fixed-point units,
- a load and store unit,
- a cache and memory unit,
- and a bus interface unit.

Additional Features

- 32-KByte L1 data cache
- 32-KByte L1 instruction cache
- up to 1-MByte L2 cache
- memory management unit (MMU) with 128 entries, two-way set-associative instruction TLB with 128 entries, two-way set-associative data TLB

3.5 L2 Cache

The PPC/PowerCoreCPCI-6750 provides an L2 cache of up to 1 MByte. The L2 cache is controlled by the L2 cache controller of the PowerPC CPU. The L2 tag is two-way set-associative with 4-K entry tags per way. Only the memory space of the processor bus devices can be cached in the L2 cache.

Data Sheet

For further information on programming the L2 cache controller see the respective *PowerPC User's Manual* available from Motorola Semiconductors.

L2 Cache Size

The available size of the L2 cache can be read by the software from the DCCR, bits [7...6].

Table 23 DCCR, Bits [7…6]

FE00.0308$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	DCCR[7…6]		DCCR[5…0]					

DCCR[7…6] DCCR[7…6] indicate the L2 cache configuration.

= 00_2 no L2 cache available

= 01_2 256-KByte L2 cache

= 11_2 512-KByte L2 cache

= 10_2 1-MByte L2 cache

DCCR[5…0] see table 24 "DCCR, Bits [5…0]" on page 43

3.6 Shared Memory

The shared memory of the board is provided by one lower memory module which is per default directly located on the board. The capacity of the shared memory may be increased by installing an upper memory module on top of the lower one.

Requirements

For detailed information on the requirements, qualified configurations, and max. power consumption of the memory modules, see section 2.1.1 “Requirements” on page 5.

Installation

For information on installing the memory module refer to the respective *Memory Module Installation Guide*.

Accessibility

The shared memory is accessible from:

- PowerPC CPU,
- other CompactPCI bus masters via the PCI-to-PCI bridge,
- Ethernet DMA controller,
- other PCI DMA controllers on PMC modules,
- or from the PCI-to-ISA bridge DMA controller.

ECC

- If an EDO DRAM memory module is installed, only ECC is supported.
- If an SDRAM memory module is installed, neither ECC nor parity is supported.

The ECC detects and corrects all single-bit errors. Double-bit errors and errors within a nibble are only detected but not corrected. ECC is enabled per default and can be disabled by the software.

Shared Memory Accesses

The following 2 different types of shared memory accesses are possible:

1. Shared memory access without ECC or parity:
   - In case of shared memory read accesses the bytes requested by the master are read from the shared memory without additional transfers for ECC or parity. If less than one long-word is read, the extraneous data is ignored by the PPC-to-PCI bridge.
   - In case of shared memory write accesses the bytes provided by the master are written into the shared memory without additional transfers for ECC or parity. If less than one long-word is written, the extraneous data is masked by control signals. Therefore, only targeted bytes are actually written.
2. Shared memory accesses with ECC

– A shared memory read access to less than one long-word is performed by the PPC-to-PCI bridge as a read access to one aligned long-word, so that the ECC byte can be checked. The 8 bytes and the ECC byte are stored in the memory controller.

– A shared memory write access to less than one long-word is performed by the PPC-to-PCI bridge as a read-modify-write access to one aligned long-word. The PPC-to-PCI bridge reads the aligned long-word, checks the ECC byte and merges the written data with the data read from the shared memory. Then the PPC-to-PCI bridge generates a new ECC for the merged long-word and writes the long-word and ECC code into the shared memory.

3.6.1 Memory Controller

The memory controller is located in the PPC-to-PCI bridge.

Memory Configuration

The memory controller registers of the PPC-to-PCI bridge are accessible via the configuration address register (CAR) and the configuration data register (CDR). For configuring the memory controller the CAR and the CDR must be set appropriately (see section 3.10 “PPC-to-PCI Bridge” on page 56).

3.6.2 Shared Memory Performance

The shared memory control logic is optimized for fast accesses from the PowerPC CPU providing the maximum performance with enabled ECC. Since the PowerPC CPU includes a data and instruction cache, many CPU accesses are cache line “burst fills”. Within four 8-byte cycles these burst fills attempt to read 32 consecutive bytes into the PowerPC CPU.

As an example the shared memory performance in case of a 66-MHz PPC bus is described in the following.

EDO DRAM Shared Memory

“8-4-4-4” Burst Transfer

If an EDO DRAM memory module is installed, the first read cycle of such a burst usually requires 8 PPC bus clock cycles. Due to the optimized design of the memory control logic, each subsequent cycle requires only 4 PPC bus clock cycles to complete. This is commonly called an “8-4-4-4” burst transfer. Overall, the total cache line “burst fill” operation requires 20 PPC bus clock cycles to transfer 32 bytes providing a maximum memory bandwidth of over 105 MByte/s at 66-MHz PPC clock frequency.

Single Read and Write

Not all CPU accesses are burst transfers. Single read and write transactions are also supported at maximum speed. A single read or write access (1, 2, 4, or 8 bytes) requires 7 PPC bus-clock cycles. Distributed asynchronous refresh is provided every 14 µs and an access during a pending refresh cycle may be delayed by a maximum of 6 additional clock cycles at 66-MHz PPC clock frequency.

SDRAM Shared Memory

"2-1-1-1" Burst Transfer

Compared to an EDO DRAM shared memory the performance increases significantly if an SDRAM memory module is installed. The first read cycle of a burst requires 2 PPC bus clock cycles. Due to the optimized design of the memory control logic, each subsequent cycle requires only 1 PPC bus clock cycle to complete. This is commonly called a "2-1-1-1" burst transfer. Overall, the total cache line "burst fill" operation requires 5 PPC bus clock cycles to transfer 32 bytes providing a maximum memory bandwidth of 528 MByte/s at 82.5-MHz PPC clock frequency.

Single Read and Write

A single read or write access (1, 2, 4, or 8 bytes) requires 3 PPC bus-clock cycles. Distributed asynchronous refresh is provided every 14.5 µs and an access during a pending refresh cycle may be delayed by a maximum of 8 additional clock cycles at 82.5-MHz PPC clock frequency.

3.6.3 Shared Memory Capacity

The capacity of the shared memory is encoded in the DCCR.

Table 24 DCCR, Bits [5…0]

FE00.0308$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	DCCR[7…6]		DCCR[5…0]					

DCCR[7…6] see table 23 "DCCR, Bits [7…6]" on page 40

DCCR[5…0] DCCR[5…0] indicate the capacity of the shared memory. All combinations not listed in the following table are reserved.

Table 25 EDO DRAM Capacity

DCCR[5…0]						Capacity [MByte]	
Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Lower EDO DRAM memory module**	**Upper EDO DRAM memory module**
don't care	don't care	0	1	1	1	16	–
don't care	don't care	1	1	0	1	64	–
don't care	don't care	1	0	0	1	64	128

Table 26 SDRAM Capacity

DCCR[5…0]						Capacity [MByte]	
Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Lower SDRAM memory module**	**Upper SDRAM memory module**
don't care	don't care	0	0	1	1	64	–
don't care	don't care	0	0	0	1	128	–
don't care	don't care	0	0	1	0	64	128
don't care	don't care	0	0	0	0	128	128

3.6.4 Shared Memory Organization

The EDO DRAM is arranged in 1 or 3 memory banks with nine 2M * 8 or 8M * 8 EDO DRAM devices in each bank.
The SDRAM is arranged in 1, 2, 3, or 4 banks with nine 8M * 8 SDRAM devices in each bank.
Each shared memory bank is 64-bit wide. The EDO DRAM memory banks provide 1 additional byte for the ECC.

3.6.5 Cache Coherency and Snooping

To maintain the cache coherency of the shared memory, the PowerPC CPU has the capability of snooping. On a snooped external bus cycle the PowerPC CPU invalidates the cache line that is hit. Snoop hits invalidate the cache line in all cases (also for alternate master read/write cycles).

3.6.6 Shared Memory Access from the PowerPC CPU

After initialization the firmware enables the complete shared memory at start address 0000.0000_{16}. The memory address range, which is accessible via the PPC bus, can be programmed in the PPC-to-PCI bridge memory controller. Depending on the shared memory capacity, the end address is set to the maximum available memory by the firmware.

Memory Modules

For information on the contiguousness of the shared memory space, see table 14 “PPC/PowerCoreCPCI-6750 Memory Map seen from the CPU” on page 30.

Table 27 Default Shared Memory Access from the PowerPC CPU

Address range	Capacity of the lower memory module [MByte]	Capacity of the upper memory module [MByte]
0000.0000_{16} ...$00FF.FFFF_{16}$	16	0
0000.0000_{16} ...$03FF.FFFF_{16}$	64	0
0000.0000_{16} ... $07FF.FFFF_{16}$	128	0
0000.0000_{16} ... $0BFF.FFFF_{16}$	64	128
0000.0000_{16} ... $0FFF.FFFF_{16}$	128	128

3.6.7 Shared Memory Access via the CompactPCI Bus

Shared memory access from the CompactPCI bus is routed by the PCI-to-PCI bridge via the local PCI bus and the PPC-to-PCI bridge. Via the PCI-to-PCI bridge the start access address and the size of the shared memory can be programmed, via the PPC-to-PCI bridge the start and end access addresses can be programmed.

Programmable Access Address Range

The access address of the shared memory for other PCI bus masters is programmable via the PCI-to-PCI bridge. The start address of the shared memory and its size are programmable in 4-KByte increments via the PCI-to-PCI bridge. Therefore, the address range used by the CompactPCI bus masters is not necessarily the same as the one used by the PowerPC CPU for local accesses.

PCI Bus Access Cycle

When the PCI-to-PCI bridge detects a CompactPCI bus access cycle to the programmed address range of the shared memory, it requests bus mastership of the local PCI bus via the PCI bus arbiter. After the arbiter has granted the PCI bus mastership to the PCI-to-PCI bridge, the PCI bus access cycle is executed and all data is latched from (read cycles) or stored to (write cycles) the shared memory. Afterwards the cycle is terminated and the PCI-to-PCI bridge keeps the PCI bus mastership until another PCI bus master requests it.

3.6.8 Shared Memory Access from the Ethernet Controller

The Ethernet controller uses the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

3.6.9 Shared Memory Access from the PMC Modules

The PMC modules may use the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

3.6.10 Shared Memory Access from the PCI-to-ISA Bridge

The PCI-to-ISA bridge uses the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

3.7 Boot Flash

Since the flash memory area is located on the PPC bus, the reset vector table in the boot flash is visible to the CPU after power-on reset before any initialization by the software. A memory address range of 2 MByte is available for the complete flash memory, i.e. for the boot flash and the user flash (see section 3.8 “User Flash” on page 50). For the boot flash the first 1-MByte range is used. If more than 1 MByte is installed, the boot flash is visible bank by bank, each bank consisting of 1 MByte. Since only 1 MByte is preserved for the boot flash bank, one additional parallel port pin provides switching techniques (see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47) to increase the boot flash capacity.

3.7.1 Boot Flash Address Range

The boot flash memory area is 8-bit wide organized. The PPC-to-PCI bridge provides 21 addressing lines to address the board flash. Therefore, 2 MByte of the complete flash address range $FFE0.0000_{16}$...$FFFF.FFFF_{16}$ are accessible for 8-bit wide organized flash devices. 1 MByte of the address space is used for the boot flash.

The following register map shows the bits provided to achieve the maximum of 2-MByte boot flash. The boot flash consists of one device with a maximum of 2 banks each consisting of 1 MByte.

Table 28 CIO: Port A Data Register, bit [5…4]

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ENA_WD	reserved	BOOT_DEV	FLSH_SEL[2]	FLSH_SEL[1…0]		reserved	FA_B[20]

ENA_WD (R/W) — see table 36 “CIO: port A Data Register, Bit [7]” on page 54

BOOT_DEV (R) — BOOT_DEV shows the selected boot device.

= 0 TSOP (J49) boot device has been selected.

= 1 PLCC (J12) boot device has been selected.

FLSH_SEL[2] (R/W) — FLSH_SEL[2] distinguishes between the 1-MByte boot flash areas of a single device. FLSH_SEL[2] is connected to the address pin A20 of the TSOP boot flash via a programmable logic device. Since the boot flash

can be accessed only between FFF0.0000$_{16}$…FFFF.FFFF$_{16}$, the software has to set FLSH_SEL[2] appropriately to select the considered 1-MByte bank. FLSH_SEL[2] extends the PPC-to-PCI bridge addressing lines and must not be changed by processor instructions fetched from the boot flash device.

FLSH_SEL [1…0] (R/W) — see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

FA_B[20] (R/W) — see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

Table 29 Boot Flash Address Range

Address range	Boot flash address space	Extended boot flash capacity via FLSH_SEL[2]
FFF0.0000$_{16}$ … FFF7.FFFF$_{16}$	512 KByte	512 KByte
FFF0.0000$_{16}$ … FFFF.FFFF$_{16}$	1 MByte	1 MByte
FFF0.0000$_{16}$ … FFFF.FFFF$_{16}$	1 MByte	2 MByte

IMPORTANT

The firmware supports commands to select the device bank which is to be mapped into the address range (see *PowerBoot User’s Manual*, section “FSELECT – Selecting Flash Memory”).

Reset Vector — The CPU reset vector is located at FFF0.0100$_{16}$.

3.7.2 Boot Flash Size and Address Map

The accessible address range of the boot flash is determined by the boot flash capacity. Therefore, the address range depends on the board type.

Table 30 Boot Flash Address Map

Boot flash		**Total boot flash capacity**	**Resulting address range for processor instructions**	**Bank address via FLSH_SEL[2]**
J49 TSOP device	**J12** PLCC device			
1 MByte	–	1 MByte	$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	0
2 MByte	–	2 MByte	$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	0…1
–	512 KByte	512 KByte	$FFF0.0000_{16}$ … $FFF7.FFFF_{16}$	0

NOTICE

The boot flash size of the PLCC devices is a factory option. Do not reduce or increase the size of the boot flash devices even if socketed. Otherwise the devices and/or data could be damaged.

3.7.3 Boot Flash Devices

The board provides one user programmable boot flash device at one of the following locations:

Location
- J49 (unsocketed)
- or J12 (socketed)

Base Address $FFF0.0000_{16}$

Device Types The available boot flash devices are programmable at VPP = 5 V.

The following table shows the boot flash factory options using the listed device types (or equivalent).

Table 31 Boot Flash Factory Options, Device Types, and Default Configuration

	Device type	**Package type**	**Default**
1.	29F040:512K * 8	PLCC (socketed)	x
2.	28F008S5:1M * 8	TSOP (unsocketed)	
3.	29F016:2M * 8	TSOP (unsocketed)	

3.7.4 Programming the Boot Flash

Writing to the boot flash is enabled only if Boot flash write protection is set to ON (default “OFF”, see page 13).

When the write protection of the boot flash is disabled, programming is handled by PowerBoot packaged with the PPC/PowerCoreCPCI-6750 (see *PowerBoot User’s Manual* “FERASE – Erasing Flash Memories” and “FPROG – Programming Flash Memories”) and by the assembly process.

NOTICE

Before erasing or programming the boot flash ensure that you do not destroy Force Computers’ firmware and make a copy of the boot flash contents.

3.8 User Flash

The second MByte of the flash memory space is used for the user flash. If more than 1-MByte user flash is installed, the user flash is visible only bankwise, each bank consisting of 1 MByte. Since only 1 MByte is preserved for the user flash bank, 3 additional parallel port pins (see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51) provide switching techniques to increase the user flash capacity. These pins extend the PPC-to-PCI bridge addressing lines.

3.8.1 User Flash Address Range

The flash memory area is 8-bit wide organized. The PPC-to-PCI bridge provides 21 addressing lines to address the flash memory. Therefore, 2 MByte of the complete flash address range $\texttt{FFE0.0000}_{16}$ … $\texttt{FFFF.FFFF}_{16}$ are accessible for 8-bit wide organized flash devices. The second 1-MByte range is used for the user flash.

The following register map shows the additional bits to be added to achieve the maximum 8-MByte user flash. The user flash can be divided into 4 flash devices each consisting of two 1-MByte banks.

Table 32 CIO: Port A Data Register, Bits [3…0]

FE00.0302							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ENA_WD	reserved	BOOT_DEV	FLSH_SEL[2]	FLSH_SEL[1…0]		reserved	FA_B[20]

ENA_WD (R/W) — see table 36 “CIO: port A Data Register, Bit [7]” on page 54

BOOT_DEV (R) — see table 40 “CIO: Port A Data Register” on page 67

FLSH_SEL[2] (R/W) — see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47

FLSH_SEL [1…0] (R/W) — FLSH_SEL[1…0] selects the user flash device to be paged into the memory range $FFE0.0000_{16}$ … $FFEF.FFFF_{16}$.

Table 33 User Alash Address Map

User flash	FLSH_SEL [1…0]	Address range
1	00_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
2	01_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
3	10_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
4	11_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$

FA_B[20] (R/W) — FA_B[20] distinguishes between the 1-MByte user flash areas of a single device. FA_B[20] is directly connected to the address pin A20 of the user flash. Since the user flash can be accessed only between $FFE0.0000_{16}$…$FFEF.FFFF_{16}$, the software has to set FA_B[20] appropriately to select the considered 1-MByte bank.

Table 34 User Alash Address Range

Address range	User flash address space [MByte]	Extended user flash capacity via FA_B[20][MByte]
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	1	1
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	1	2

IMPORTANT

The firmware supports commands to select the device bank to be mapped into the address range (see *PowerBoot User's Manual*, section "FSELECT – Selecting Flash Memory").

3.8.2 User Flash Size

The on-board user flash is accessible according to table 33 "User Alash Address Map" on page 51. The following user flash capacities are available:

- 0 MByte
- 4 MByte if
  - four 1M * 8 devices
  - or two 2M * 8 devices are used
- 8 MByte if four 2M * 8 devices are used

3.8.3 User Flash Devices

The user flash consists of up to 4 user programmable devices.

Base Address $FFE0.0000_{16}$

Device Types The available boot flash devices are programmable at VPP = 5 V.

The following table shows the factory options available for the user flash using the device types listed (or equivalent).

Table 35 User Flash Device Types (Factory Options) and Address Ranges

	Device type	Number	Address range
1.	No user flash installed		
2.	28F008S5:1M * 8	4	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
3.	29F016:2M * 8	4	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$

3.8.4 Programming the User Flash

Writing to the user flash is enabled only if SW6-3 is set to OFF (default “OFF”, see page 13).

When the write protection of the user flash is disabled, programming is handled by PowerBoot packaged with the PPC/PowerCoreCPCI-6750 (see *PowerBoot User’s Manual* section “FERASE – Erasing Flash Memories” and section “FPROG – Programming Flash Memories”) and by the assembly process.

3.9 Watchdog Timers

The PPC/PowerCoreCPCI-6750 provides 2 independent watchdog timers monitoring the CPU activity. If no triggering occurs during the selected timeout periods,

- the watchdog timer 1 generates a reset pulse
- and the watchdog timer 2 generates an NMI or a high-level interrupt (depending on the setting of SW8-4) to the PowerPC CPU.

Enabling the Watchdog Timers

- The watchdog timer 1 is enabled by setting SW8-1 to ON (default “OFF = disabled”, see page 14).
- The watchdog timer 2 is enabled by setting SW8-2 to ON (default “OFF = disabled”, see page 14).

Starting the Watchdog Timers

If SW8-1 and SW8-2 are set appropriately, both watchdog timers will be started via `ENA_WD` in the CIO: port A Data Register, Bit [7]. When start-

ed, the watchdog timers can be stopped only by a reset. After a reset none of the watchdog timers is started.

Table 36 CIO: port A Data Register, Bit [7]

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ENA_WD	reserved	BOOT_DEV	FLSH_SEL [2]	FLSH_SEL[1…0]		reserved	FA_B[20]

ENA_WD (R/W)

ENA_WD starts the watchdog timers 1 and 2.

= 0 Watchdog timers 1 and 2 are started if low level is held for more than 8 ms.

= 1 no change

BOOT_DEV (R)

see table 40 “CIO: Port A Data Register” on page 67

FLSH_SEL[2] (R/W)

see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47

FLSH_SEL [1…0] (R/W)

see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

FA_B[20] (R/W)

see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

Triggering

A watchdog timer is triggered when the respective sanity check of this timer is performed. A sanity check includes 2 write cycles to the appropriate sanity check address with defined data. After the sanity check has been performed, the timeout period for the watchdog timer will be reset.

Watchdog Timer 1

To trigger the watchdog timer 1, take the following 2 steps:

1. Write 55_{16} to the ISA I/O address 312_{16}.
2. Write AA_{16} to the ISA I/O address 312_{16}.

Watchdog Timer 2

To trigger the watchdog timer 2, take the following 2 steps:

1. Write 55_{16} to the ISA I/O address 316_{16}.
2. Write AA_{16} to the ISA I/O address 316_{16}.

NOTICE

Although the watchdog timers are started synchronously, they may be re-triggered independently, hence asynchronously. Thus, it is possible to get a reset pulse from the watchdog timer 1 without gotten an interrupt from the watchdog timer 2 (if both watchdog timers are enabled). In order to

avoid this, the sanity checks for both timers should be performed simultaneously.

Timeout — The watchdog timeout period can be selected via SW8-3 (see table 8 “Default Switch Settings” on page 13).

Interrupt — If triggering of the watchdog timer 2 does not occur within the selected watchdog timeout period, the watchdog timer 2 asserts an interrupt to the PCI-to-ISA bridge:

- If SW8-4 is set to ON, an IOCHCK interrupt, which is an NMI, is asserted and routed to the MCP# interrupt pin of the PowerPC CPU.
- If SW8-4 is set to OFF, an ISA_IRQ<8># interrupt is asserted which is routed to the shared interrupt input of the PowerPC CPU.

Reset — If triggering of the watchdog timer 1 does not occur within the selected watchdog timeout period, the watchdog timer 1 initiates a reset of the board.

BSCR: Watchdog Status Register — The PPC/PowerCoreCPCI-6750 provides a BSCR watchdog status register indicating the current watchdog parameters. The register bits 3…0 reflect the setting of SW8-4, SW8-3, SW8-2, and SW8-1.

Table 37 BSCR: Watchdog Status Register, Bits [4…0]

$FE00.0320_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	reserved	reserved	reserved	WD started	WD2 routing	WD timeout	WD2 enable	WD1 enable

WD started (R) — WD started indicates whether the watchdog timers 1 and 2 have been started via ENA_WD (see table 36 “CIO: port A Data Register, Bit [7]” on page 54).

= 0 Watchdog timers 1 and 2 have not been started.

= 1 Watchdog timers 1 and 2 have been started.

WD2 routing (R) — WD2 routing indicates the interrupt type generated by the watchdog timer 2.

= 0 Watchdog timer 2 generates a high-level interrupt (SW8-4 set to ON).

= 1 Watchdog timer 2 generates an NMI (SW8-4 set to OFF).

WD timeout (R) — WD timeout indicates the period of time after which the watchdog time of the watchdog timers 1 and 2 expires. When the selected time of the watchdog timers 1 and 2 has expired, a reset of the board and an NMI, respectively, are going to be generated.

= 0 Watchdog timer 1 expires after ~2,5 s

and watchdog timer 2 expires after ~ 500 ms (SW8-3 set to ON).

= 1 Watchdog timer 1 expires after ~0,5 s
and watchdog timer 2 expires after ~ 32 ms (SW8-3 set to OFF).

WD2 enable (R) — WD 2 enable indicates whether the watchdog timer 2 is enabled.

= 0 Watchdog timer 2 is disabled (SW8-2 set to ON).

= 1 Watchdog timer 2 is enabled (SW8-2 set to OFF).

WD1 enable (R) — WD 1enable indicates whether the watchdog timer 1 is enabled.

= 0 Watchdog timer 1 is disabled (SW8-1 set to ON).

= 1 Watchdog timer 1 is enabled (SW8-1 set to OFF).

3.10 PPC-to-PCI Bridge

The PPC-to-PCI bridge provides an integrated and PowerPC compliant interface between the PowerPC CPU, the main memory, the user and boot flash, and the PCI bus.

Processor Interface

The processor interface provides a 64-bit data bus and a 32-bit address bus. It supports full memory coherency. Furthermore, it pipelines processor accesses.

Memory Interface

Depending on the memory module installed on the board, the memory interface is programmed to support the shared memory. The memory interface provides a 64-bit data bus to the shared memory. If an EDO DRAM memory module is installed on the board, ECC is per default enabled by the software (see section 3.6 “Shared Memory” on page 41). The PPC-to-PCI bridge supports up to 1-GByte shared memory.
The memory interface supports writing of flash memory and write buffering for PCI and processor accesses.

Features of the PCI Interface

The PCI interface implements the following features:

- compliant with the *PCI Local Bus Specification Rev. 2.1*
- operation at 33 MHz
- PCI interlocked accesses to shared memory via lock pin and lock protocol
- accesses to all PCI address spaces
- selectable big or little endian operation

- store gathering of PPC-to-PCI writes and PCI-to-memory writes and memory prefetching of PCI read accesses
- PCI configuration registers
- data buffering (in/out)
- parity support
- error reporting mechanism
- concurrent transactions on the processor and the PCI bus

Registers

The register set of the PPC-to-PCI bridge is accessible via the configuration address register (CAR) and the configuration data register (CDR). To configure the memory controller, the CAR and the CDR must be set appropriately:

- To access the register set of the PPC-to-PCI bridge with offset xy, the CAR must contain $xy00.0080_{16}$ (see table 17 “PPC/PowerCoreCPCI-6750Configuration Base Addresses” on page 32). The register offset xy has to be written into the most significant byte of the CAR. The lowest significant byte must be set to 80_{16} (swapped byte).
- The CDR contains the contents for the memory controller registers (R/W) to be accessed.

Table 38 CAR and CDR address map

Register	Address
CAR	$FEC0.0000_{16}$
CDR	$FEE0.0000_{16}$

Example

If you want to enable memory bank 0 and 1, you have to access the memory bank enable register at offset $A0_{16}$, and to write the value 03_{16} into this register:

1. Write the value $A000.0080_{16}$ to the CAR address $FEC0.0000_{16}$.
2. Write the value 03_{16} to the CDR address $FEE0.0000_{16}$.

3.11 PCI-to-PCI Bridge

The PCI-to-PCI bridge may act as PCI master and PCI slave device on the CompactPCI bus and is particularly convenient for the local PCI bus.

Features

The PCI-to-PCI bridge provides:

- 32-bit with up to 33-MHz PCI bus interface on the CompactPCI bus and the local PCI bus
- integral buffers for write posting and read buffering to maximize bandwidth utilization
- 2 sets of standard PCI configuration registers:
  - one set for the CompactPCI bus
  - and one for the local PCI bus.
- 4 programmable interface base address configuration registers for downstream forwarding from CompactPCI to local PCI and 3 programmable interface base address configuration registers for upstream forwarding from local PCI to CompactPCI
- flexible register set programmable from the CompactPCI bus and the local PCI bus (not valid for the CSR register sets)

CSR Base Address

- For the local PCI interface the CSR base address is set by the user (CSR base address + 4 KByte).
- For the CompactPCI interface the CSR base address is set by the CompactPCI system controller.

3.11.1 CompactPCI Bus Interface

The PPC/PowerCoreCPCI-6750 provides a complete CompactPCI bus interface compliant with the *CompactPCI Specification PICMG 2.0 R2.1*.

BARs

The PCI-to-PCI bridge includes 4 base address registers (BARs) to perform downstream transfers from the CompactPCI bus to the local PCI bus:

- BAR 0: used for mapping downstream memory space and the lower 4 KByte of the CompactPCI CSR space
- BAR 1: used for mapping downstream memory or I/O space
- BAR 2: used for mapping downstream memory space
- BAR 3: used for mapping downstream memory space

The size of the BARs can be programmed and may also be disabled. Only BAR 0 cannot be disabled, since the CSRs for the CompactPCI bus are always mapped into this area.

Supported Transfers

The CompactPCI bus interface responds to the following transfers:

- all memory commands
- I/O read and write commands
- dual address commands
- type 0 configuration commands

The CompactPCI bus interface is able to initiate the following transfers:

- all memory commands
- I/O read and write commands
- dual address commands
- type 0 and type 1 configuration commands

3.11.2 Local PCI Bus Interface

The PPC/PowerCoreCPCI-6750 provides a complete local PCI bus interface compliant with the *PCI Local Bus Specification Rev. 2.1*.

BARs

The PCI-to-PCI bridge includes 3 BARs to perform upstream transfers from the local PCI bus to the CompactPCI bus. 2 of them are used for mapping upstream memory space. The third BAR may be programmed for I/O or memory space mapping:

- BAR 0: used for mapping upstream memory or I/O space
- BAR 1: used for mapping upstream memory space
- BAR 2: used for mapping upstream memory space

The size of the BARs can be programmed and may also be disabled.

Supported Transfers

The local PCI bus interface responds to the following transfers:

- all memory commands
- I/O read and write commands
- dual address commands
- type 0 configuration commands

The local PCI bus interface is able to initiate the following transfers:

- all memory commands

- I/O read and write commands
- dual address commands
- type 0 and type 1 configuration commands

3.11.3 Exception Signals

The *PCI Local Bus Specification Rev. 2.1* includes the signals INTA#, INTB#, INTC#, and INTD# for signalling exceptions or status.

CompactPCI Interrupt

On the CompactPCI bus the signal INTA# is connected to the backplane and forwards an exception signal to the system board (board in the system slot).

A CompactPCI interrupt is going to be asserted when one of the following conditions is true:

- The appropriate doorbell register bit is set.
- The I2O outbound queue is not empty.
- The subsystem event bit is set.

These conditions are individually maskable.

Local PCI Interrupt

On the local PCI bus the signal INTA# is connected to the CPU via the interrupt handler located in the PCI-to-ISA bridge and the PPC-to-PCI bridge.

A local PCI interrupt is asserted when one of the following conditions is true:

- The appropriate doorbell register bit is set.
- The I2O inbound queue is not empty.
- A page boundary is reached when performing lookup table address translation.

These conditions are individually maskable.

3.12 Ethernet Interface

The PPC/PowerCoreCPCI-6750 offers a Local Area Network (LAN) interface at the front panel. This LAN interface is based on

- an Ethernet controller located at the PCI bus
- an Ethernet interface adapter

- and on a filter transformer routing the 2 differential receive and the 2 differential transmit lines of the 10Base-T or 100Base-TX interface to the Ethernet interface adapter.

Ethernet Address

The unique Ethernet address is permanently stored at the ID-ROM (see section 2.9 “Ethernet Interface” on page 18). After power-on the Ethernet address is copied into the NVRAM at offset $1C12_{16}$ where it can be read by the software.

Features

The Ethernet interface provides the following features:

- compatibility with IEEE 802.3/Ethernet
- data rate of 100 Mbit/s
- DMA capability
- interrupt generation

3.12.1 Ethernet Controller

The fast Ethernet LAN controller provides the following features:

Integration Features

- integration features
  - integrated PCS and scrambler/descrambler for CAT5
  - integrated AUI port routed to PN15, which is a factory option (see figure 4 “PN15 Connector Pinout” on page 22), and to J5 of the CompactPCI bus (see figure 3 “Pinout of the CompactPCI Connector J5, Rows A…E” on page 20)
  - autonegotiation of full-duplex and half-duplex operation for 10 and 100 Mbit/s (NWAY)

Performance Features

- performance features
  - support of PCI read multiple, read line, and write and invalidate commands
  - direct shared memory access (DMA) with programmable burst size provided for low CPU utilization
  - unlimited PCI burst support
  - support of early interrupt on transmitting and receiving
  - support of a variety of flexible address filtering modes (including perfect, hash tables, inverse perfect, and promiscuous)

Device Features
- device features
  - support of big or little endian byte ordering for buffers and descriptors
  - support of full-duplex operation on MII port
  - low-power management with 2 power-saving modes (sleep and snooze)
  - internal and external loopback capability on all network ports
  - LED support for network activity indications
  - low-power, 3.3-V CMOS technology
  - maximum supply current after power-up: 70 mA

Automatic Detection and Sensing Features
- automatic detection and sensing features
  - support of the IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex operation for 10 and 100 Mbit/s

CSR Base Address
The CSR base address of the Ethernet controller is $\texttt{FE85.0000}_{16}$.

Interrupt
The Ethernet controller uses the signal INTB# for interrupting the CPU (see table 20 “Default PPC/PowerCoreCPCI-6750 Interrupt Map” on page 35).

3.12.2 Ethernet Interface Adapter

Features
The Ethernet interface adapter integrates:
- physical layer integrated in one device
- MII interface
- 10Base-T and 100Base-TX compliant half- and full-duplex transceiver
- extended register set including detailed status monitoring

3.13 PCI-to-ISA Bridge

Master/Slave Interfaces
The PCI-to-ISA bridge provides:
- a PCI master/slave interface with 33 MHz
- and an ISA master/slave interface with 8.25 MHz.

Timer/Counter	The PCI-to-ISA bridge integrates a timer/counter with 3 channels.
Interrupt Controller	In addition, the PCI-to-ISA bridge includes 2 interrupt controllers supporting 15 interrupt channels. These interrupt controllers can be programmed independently of edge or level sensitivity.
DMA Functions	The PCI-to-ISA bridge has 2 DMA controllers and 7 independently programmable channels.
NMIs	The PCI-to-ISA bridge integrates a control logic generating NMIs.
Multifunctional Device	The PCI-to-ISA bridge is a multi-functional device: • the PCI-to-ISA bridge is function 0, • the IDE controller (not used on the board) is function 1. Both functions can be configured independently. The IDE interface is disabled per default.

3.13.1 PCI-to-ISA Function

The PCI-to-ISA-bridge prevents the slower I/O devices from slowing down the PCI bus.

Devices and Registers on the ISA bus	The following devices/registers are located on the ISA bus: • 2 serial interfaces • NVRAM and RTC • CIO for internal control • DCCR • BSCRs • PN15 connector (factory option) for ISA extension
ISA Base Address	The ISA base address of the PCI-to-ISA bridge is $\texttt{FE00.0000}_{16}$.

3.13.2 Interrupt Controller

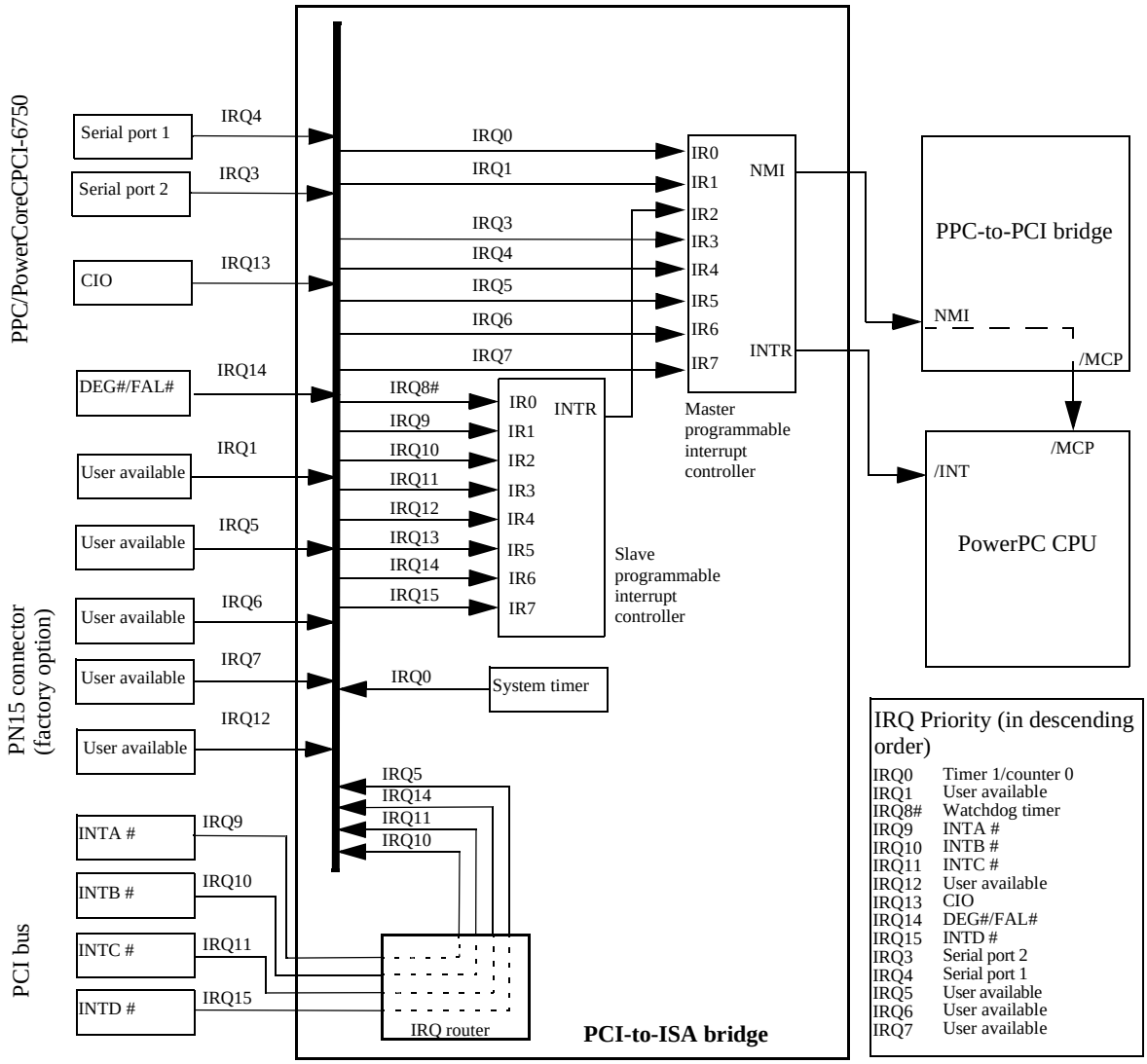
The following figure shows the default interrupt structure of the CPU board. The interrupt controller of the PCI-to-ISA bridge is used for interrupt routing. The PCI-to-ISA bridge collects the possible interrupts

and passes them to the CPU via the INTR line. An NMI is generated only if:

- a PCI system error (PCI signal SERR# active) occurs,
- a watchdog timeout occurs,
- or the Abort key is pressed.

All interrupts can be disabled independently.

Figure 6 Default PCI-to-ISA Bridge Interrupt Structure



3.14 Real-Time Clock / Non-Volatile RAM

The real-time clock (RTC) and the non-volatile RAM (NVRAM) are housed in one device including a battery backup.

Features of the Battery

The battery is mounted as snaphat on top of the device with a direct connection to its power supply. For information on exchanging the battery see section 2 “Installation” on page 5.
If the power fails, the device is automatically deselected and changes into write-protected mode.

Address Space

The RTC/NVRAM address space is divided into 3 used parts.

Table 39 Address Ranges of the RTC/NVRAM

Address range	Access
0000_{16} … $1BFF_{16}$	NVRAM user defined area
$1C00_{16}$ … $1FF0_{16}$	NVRAM configuration area
$1FF1_{16}$ … $1FF7_{16}$	unused
$1FF8_{16}$ … $1FFF_{16}$	RTC registers

Address Access

The access to the RTC/NVRAM is 8-bit wide and indirect. To access a location within the device:

1. write the lower address byte to $FE00.0073_{16}$ (write-only),
2. write the higher address byte to $FE00.0075_{16}$ (write-only),
3. and read or write data from or to $FE00.0077_{16}$.

NVRAM

Since the last 16 bytes are used for the RTC or unused, the NVRAM has a capacity of 8 KByte – 16 bytes. The complete address space of the NVRAM is 0000_{16} … $1FF0_{16}$.

User Defined Area

The user may store important data in the user defined area of the NVRAM.

Configuration Area

The NVRAM configuration area is used for internal configuration data.

IMPORTANT Do not change the values stored in the configuration area.

Features of the RTC

The on-board RTC maintains accurate time and date based on its own quartz. The on-board RTC is year-2000 compliant.

3.15 PPC/PowerCoreCPCI-6750 Parameters, Timers, and CIO

The configuration and status information for several PPC/PowerCoreCPCI-6750 parameters and timers are accessible via an 8-bit register, the CIO data and timer registers, and the NVRAM configuration area. They are all located on the ISA bus.

3.15.1 Parameters

Some of the following parameters can only be read, others can be read and written:

– DRAM — reading the DCCR (see table 24 “DCCR, Bits [5…0]” on page 43)

– Cache — reading the DCCR (see table 23 “DCCR, Bits [7…6]” on page 40)

– Boot flash — writing parameters of the boot flash devices via CIO port A (see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47)

– User flash — writing parameters of the user flash devices via CIO port A (see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51)

– Boot parameters — reading the boot parameters from the NVRAM (see section 3.14 “Real-Time Clock / Non-Volatile RAM” on page 65)

– ID-ROM — The ID-ROM includes different parameters internally used.

– Busmode — The PMC busmode signals can be set and read via CIO port B (see table 49 “CIO: Port B Data Register, Bits [5...1]” on page 75).

3.15.2 Timers

The PPC/PowerCoreCPCI-6750 includes 5 different timers:

- The PowerPC CPU provides a 64-bit timer.
- The PCI-to-ISA bridge provides a system timer (counter 0, IRQ 0).
- The CIO provides 3 independently programmable 16-bit timers with 500-ns resolution which can also be used as counters.

The peripheral clock of the CIO device is connected to a 4.125-MHz source.

3.15.3 CIO

The PPC/PowerCoreCPCI-6750 integrates 1 CIO which controls internal signals and devices. The CIO includes 3 independently programmable ports A, B, and C.

Features of the CIO

The CIO contains:

- 2 independent 8-bit ports (ports A and B),
- one special-purpose 4-bit port (port C),
- and 3 independently programmable 16-bit timers which can also be used as counters.

Base address

$FE00.0300_{16}$

IRQ

The interrupt request output of the CIO uses IRQ13.

3.15.4 CIO: Port A Data Register

Table 40 CIO: Port A Data Register

$FE00.0302_{16}$							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ENA_WD	reserved	BOOT_DEV	FLSH_SEL [2]	FLSH_SEL [1…0]		reserved	FA_B[20]

ENA_WD (R/W)

see table 36 “CIO: port A Data Register, Bit [7]” on page 54

BOOT_DEV (R)

see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47

FLSH_SEL[2] (R/W)

see table 28 “CIO: Port A Data Register, bit [5…4]” on page 47

FLSH_SEL [1…0] (R/W)

see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

FA_B[20] (R/W) — see table 32 “CIO: Port A Data Register, Bits [3…0]” on page 51

3.15.5 CIO: Port B Data Register

Table 41 CIO: Port B Data Register, Bits [7…6]

FE00.0301$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ID_SCL	ID_SDA	BUSMODE[4…2]			BUSMODE[1…0]		ISA_IDENT

ID_SCL (W) — ID_SCL controls the ID-ROM SCL signal (I^2C bus).

ID_SDA (R/W) — ID_SDA controls and indicates the status of the ID-ROM serial data signal (I^2C bus).

BUSMODE [4…2] (R/W) — see table 49 “CIO: Port B Data Register, Bits [5...1]” on page 75

BUSMODE [1…0] (R) — see table 49 “CIO: Port B Data Register, Bits [5...1]” on page 75

ISA_IDENT (R) — see table 50 “CIO: Port B Data Register, Bit [0]” on page 76

3.15.6 CIO: Port C Data Register

Table 42 CIO: Port C Data Register, Bits [3…0]

FE00.0300$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	used as masking bits for write accesses to bit 3…0 (e.g.: if bit 4 is 1, bit 0 cannot be written)				LED[3…2]		LED [1…0]	

LED[3…2] (R/W) LED[3…2] controls the user LED U2 at the front panel.

= 00_2 User LED U2 is off.

= 01_2 User LED U2 is green.

= 10_2 User LED U2 is red.

= 11_2 User LED U2 is off (default).

LED[1…0] (R/W) LED[1…0] controls the user LED U1 at the front panel.

= 00_2 User LED U1 is off.

= 01_2 User LED U1 is green.

= 10_2 User LED U1 is red.

= 11_2 User LED U1 is off (default).

3.16 Board Status and Capability Registers - BSCRs

The PPC/PowerCoreCPCI-6750 provides several BSCRs. These registers indicate the current status of the board and include features for generating software requested reset conditions.
All BSCRs are located on the ISA bus and are accessible in the address range $FE00.0312_{16}$…$FE00.0340_{16}$. Unused addresses within this address range are reserved.

3.16.1 BSCR: Watchdog Timer 1 Sanity Check Register

Table 43 BSCR: Watchdog Timer 1 Sanity Check Register, Bits [7…0]

$FE00.0312_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ISA_DATA[7…0]							

ISA_DATA[7…0] (W) ISA_DATA[7…0] correspond to the part of the sanity check which is performed.
2 write accesses are required to retrigger the watchdog timer 1.

= 55_{16} 1st part of sanity check is performed.

= AA_{16} 2nd part of sanity check is performed.

3.16.2 BSCR: Watchdog Timer 2 Sanity Check Register

Table 44 BSCR: Watchdog Timer 2 Sanity Check Register, Bits [7…0]

FE00.0316$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ISA_DATA[7…0]							

ISA_DATA [7…0] (W)

ISA_DATA[7…0] correspond to the part of the sanity check which is performed.
2 write accesses are required to retrigger the watchdog timer 2.

= 55_{16} 1st part of sanity check is performed.

= AA_{16} 2nd part of sanity check is performed.

3.16.3 BSCR: Watchdog Status Register

Table 45 BSCR: Watchdog Status Register, Bits [4…0]

FE00.0320$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	reserved			WD started	WD2 routing	WD timeout	WD2 enable	WD1 enable

WD started (R)
WD2 routing (R)
WD timeout (R)
WD2 enable (R)
WD1 enable (R)

see table 37 “BSCR: Watchdog Status Register, Bits [4…0]” on page 55

3.16.4 BSCR: Last Reset Register

In the last reset register only one bit is set at time. This bit indicates the last reset source. The bits have different priorities: if more than one reset source is active, bit 0 has the highest, bit 7 the lowest priority.

Only the reset sources described in the following are indicated by the last reset register. If the reset is generated by another source, the last reset register does not indicate this source and keeps its current value.

Table 46 BSCR: Last Reset Register, Bits [7…5] and [2…0]

$FE00.0324_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	pbrst	soft_ rst	sw_rst_ req	reserved		wd_ expired	rst_ switch	power_ up

pbrst (R) — pbrst indicates whether the last reset has been generated by the signal PBRST# asserted to the CompactPCI backplane.

= 0 Last reset has not been generated by PBRST# asserted to the CompactPCI backplane.

= 1 Last reset has been generated by PBRST# asserted to the CompactPCI backplane.

soft_rst (R) — soft_rst indicates whether the last reset has been generated by a soft reset signal to the processor.

= 0 Last reset has not been generated by a soft reset.

= 1 Last reset has been generated by a soft reset.

sw_rst_req (R) — sw_rst_req indicates whether the last reset has been generated via access to the Reset request register (see table 47 “BSCR: Reset Request Register, Bits [7…0]” on page 73).

= 0 Last reset has not been generated by software.

= 1 Last reset has been generated by software.

wd_expired (R) — wd_expired indicates whether the last reset has been generated due to the expired timeout period of the watchdog timer 1.

= 0 Last reset has not been generated due to the expired timeout of watchdog timer 1.

= 1 Last reset has been generated due to the expired timeout of watchdog timer 1.

rst_switch (R) — rst_switch indicates whether the last reset has been generated via the front-panel Reset key.

= 0 Last reset has not been generated via front-panel Reset key.

= 1 Last reset has been generated via front-panel Reset key.

power_up (R) — power_up indicates whether the last reset has been generated via a power-up of the board.

= 0 Last reset has not been generated by powering up the board.

= 1 Last reset has been generated by powering up the board.

3.16.5 BSCR: Reset Request Register

Table 47 BSCR: Reset Request Register, Bits [7…0]

FE00.0332$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ISA_DATA[7…0]							

ISA_DATA [7…0] (W) ISA_DATA[7…0] correspond to the kind of reset requested by the software.

- = 11_{16} Hard reset of the board is requested.
- = 22_{16} Soft reset of the processor is requested.
- = 44_{16} PBRST# is asserted to the CompactPCI backplane.
- = 88_{16} PBRST# is deasserted to the CompactPCI backplane.

3.17 Serial I/O Ports – SCCs

The PPC/PowerCoreCPCI-6750 provides 2 serial I/O ports implemented by 2 serial communication controllers (SCCs).

Features The SCCs

- run with all existing 16C450 software
- and provide
  - programmable baudrate generator,
  - standard asynchronous communication bits,
  - and fully programmable serial interface characteristics.

Clock Input The peripheral clock input of the SCCs is driven by an 1.8-MHz clock.

IRQs The interrupt requests of the SCCs are connected to the IRQ4 and IRQ3 input of the PCI-to-ISA-bridge.

Table 48 SCC Base Addresses

Serial I/O port	SCC base address
1	FE00.03F8$_{16}$
2	FE00.02F8$_{16}$

RS-232 interfaces

The serial I/O interfaces are implemented as RS-232 interfaces. They are available at the front panel.

Connector Pinout

For information on the connectors at the front panel and the connectors' pinout see section 2.7 "Serial I/O Ports" on page 16.

3.18 PMC Slots

The PPC/PowerCoreCPCI-6750 provides 2 PMC slots.

Power and Requirements

For detailed information on the power and the requirements of the PMC modules see section 2.1 "Installation Prerequisites and Requirements" on page 5 and section 2.12 "PMC Slots" on page 21.

3.18.1 Busmode

Via the signals BUSMODE[4…2] and BUSMODE[1…0] the host gets information on:

- the presence of PMC modules (= card)
- and the logical protocol of the PMC modules.

Via the BUSMODE[4…2] signals driven by the host the PMC modules get the information whether a host is present. The answer of the PMC modules is transferred by the signal lines BUSMODE[1…0].

IMPORTANT

The BUSMODE[4…2] signals must be set accordingly. If port B is not initialized, the PMC modules do not detect the host and do not work. Per default, the firmware initializes the signals BUSMODE[4…2].

Table 49 CIO: Port B Data Register, Bits [5...1]

FE00.0301$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ID_SCL	ID_SDA	BUSMODE[4…2]			BUSMODE1…0]		ISA_ IDENT

ID_SCL (W) — see table 41 “CIO: Port B Data Register, Bits [7…6]” on page 68

ID_SDA (R/W) — see table 41 “CIO: Port B Data Register, Bits [7…6]” on page 68

BUSMODE [4…2] (R/W) — BUSMODE[4…2] indicate the meaning of the 3 output signals BUSMODE [4…2] routed to both PMC slots.

- = 000_2 Card Present Test: The cards at PMC slots 1 and 2 return "Card Present" if they are plugged into the slot and no bus protocol is used.
- = 001_2 Card Present Test: The cards at PMC slots 1 and 2 return "Card Present" if they are PCI capable and PCI protocol is used (default).
- = 010_2 Card Present Test: The cards at PMC slots 1 and 2 return "Card Present" if they are SBus capable and SBus protocol is used.
- = 011_2 reserved
- = 100_2 reserved
- = 101_2 reserved
- = 110_2 reserved
- = 111_2 no host present

BUSMODE [1…0] (R) — The PMC cards indicate their presence to the given protocol (e.g. PCI protocol, SBus protocol) by the message "Card present". BUSMODE[1] is connected to the PMC slot 2, BUSMODE[0] to the PMC slot 1.

- = 0 card present
- = 1 no card present

ISA_IDENT (R) — see table 50 “CIO: Port B Data Register, Bit [0]” on page 76

3.19 ISA Devices

The connector PN15, which is a factory option, may be used to install ISA devices.

Table 50 CIO: Port B Data Register, Bit [0]

$FE00.0301_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ID_SCL	ID_SDA	BUSMODE[4…2]			BUSMODE1…0]		ISA_ IDENT

ID_SCL (W) — see table 41 “CIO: Port B Data Register, Bits [7…6]” on page 68

ID_SDA (R/W) — see table 41 “CIO: Port B Data Register, Bits [7…6]” on page 68

BUSMODE [4…2] (R/W) — see table 49 “CIO: Port B Data Register, Bits [5...1]” on page 75

BUSMODE [1…0] (R) — see table 49 “CIO: Port B Data Register, Bits [5...1]” on page 75

ISA_IDENT (R) — ISA_IDENT indicates whether ISA devices are installed at the PN15 connector (see figure 4 “PN15 Connector Pinout” on page 22).

- = 0 ISA devices installed
- = 1 no ISA devices installed (default)

Please Note…

The *PowerBoot User's Manual* is an integral part of the *PPC/PowerCoreCPCI-6750 Technical Reference Manual* (P/N 211344), which is packaged separately.

The *PowerBoot User's Manual* will always be shipped together with the *Technical Reference Manual*.

Please:

☞ **Insert the *PowerBoot User's Manual* (P/N 204525) now into the *PPC/PowerCoreCPCI-6750 Technical Reference Manual* (P/N 211344).**

☞ **Remove this sheet.**

4 PowerBoot (= PowerBoot User’s Manual)

5 PowerBoot for PPC/PowerCoreCPCI-6750

This chapter describes the board specific PowerBoot commands.

Command Overview

PowerBoot includes the following board specific commands:

- command to manually map the PCI bus devices at the PMC slot 1 or 2:

  “PMCPCI – Mapping PMC Modules” on page 83,

- command to restart the CPU board:

  “RESET – Restarting the Board” on page 85,

- command to set and display auto boot after power-on:

  “SETBOOT – Editing Auto Boot Parameters” on page 86,

- command to turn the user LED at the front panel ON or OFF:

  “USERLED – Setting User LED” on page 95.

Supports and Requirements

PowerBoot supports up to 9-MByte on-board flash memory:

- 1-MByte boot flash for PowerBoot, OpenFirmware, or other operating systems, which can always be accessed,
- and an 8-MByte user flash which can be accessed in 8 windows each consisting of 1 MByte.

The PowerBoot flash memory must be located at the CPU address $\texttt{FFF0.0000}_{16}$, because the PPC/PowerCoreCPCI-6750 CPU vectors to the address $\texttt{FFF0.0100}_{16}$ after releasing an active /RESET. Additionally, this flash memory has to be visible to the CPU at all times (no bank switching).

5.1 PPC/PowerCoreCPCI-6750 Address Map

The following table lists the default addresses of the PPC/PowerCoreCPCI-6750 board mapped by PowerBoot.

Table 51 PPC/PowerCoreCPCI-6750 Address Map Seen from the CPU

Address	Device	
0000.0000_{16} … $3FFF.FFFF_{16}$	EDO DRAM or SDRAM:	memory modules
4000.0000_{16} … $7FFF.FFFF_{16}$	PowerPC-to-PCI bridge	
8000.0000_{16} … $FDFF.FFFF_{16}$	PCI memory	
$FE00.0000_{16}$	PCI-to-ISA bridge:	base address of ISA registers
$FE00.0073_{16}$	ISA RTC/NVRAM:	low-address byte port
$FE00.0075_{16}$		high-address byte port
$FE00.0077_{16}$		data byte port
$FE00.0300_{16}$ … $FE00.0303_{16}$	CIO parallel port addresses	
$FE00.0308_{16}$	DCCR	
$FE00.0310_{16}$	Chip select signal (PN15 connector)	
$FE00.03F8_{16}$ … $FE00.03FF_{16}$	Serial console:	I/O port
$FE85.0000_{16}$	Ethernet controller:	base address of CSR registers
$FE86.0000_{16}$	PCI-to-PCI bridge	base address of CSR registers
$FEC0.0000_{16}$	PCI bus:	configuration address register (CAR)
$FEE0.0000_{16}$		configuration data register (CDR)
$FEF0.0000_{16}$	Interrupt acknowledge cycle	
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash:	window for devices 1, 2, 3, 4
$FFF0.0000_{16}$ … $FFF7.FFFF_{16}$	Boot flash (default: 512 KByte):	device 1
$FFF0.0000_{16}$ …$FFFF.FFFF_{16}$	Boot flash (fact. opt.: 1 MByte):	device 1

5.2 PMCPCI – Mapping PMC Modules

PMCPCI manually maps a user mounted PMC module to any location in the PCI addressing space by defining its PCI I/O space address and/or its PCI memory space address. The PCI addressing space is divided into 2 areas:

Table 52 PCI Addressing Spaces

PCI addressing space	Address	PCI addressing space seen from the
PCI I/O space	$FE80.0000_{16}$ …$FEBF.FFFF_{16}$	CPU
	0080.0000_{16} …$00BF.FFFF_{16}$	PCI bus master
PCI memory space	8000.0000_{16} …$FCFF.FFFF_{16}$	CPU or PCI bus master

On the PPC/PowerCoreCPCI-6750 the CSR registers for the local Ethernet device and the PCI-to-PCI bridge are already mapped to the PCI I/O space (see table 51 “PPC/PowerCoreCPCI-6750 Address Map Seen from the CPU” on page 82).

Syntax

PMCPCI *PmcModule PciIOSpaceAddr PciMemSpaceAddr*

PmcModule
defines the PMC module to be mapped:

– 1 = PMC module 1

– 2 = PMC module 2

PciIOSpaceAddr
defines the PCI I/O space address seen from the PCI bus. If the PCI I/O space address is set to 0000.0000_{16}, it will be ignored.

PciMemSpaceAddr
defines the PCI memory space address seen from the PCI bus. If the PCI memory space address is set to 0000.0000_{16}, it will be ignored.

Description

PMCPCI checks the capabilities of every device.

- If the PCI device mounted on a PMC module supports both addressing spaces, the PCI bus device register at offset 10_{16} is used for the PCI I/O space and the PCI bus device register at offset 14_{16} is used for the PCI memory space. In this case both addresses given by the user are programmed in the PCI bus device.

- If a PCI bus device mounted on a PMC module does not support both addressing spaces, only the supported one will be used even if both addressing spaces have been defined.
- If a PCI bus device mounted on a PMC module is able to support both addressing spaces, but only one should be used, set the address not to be used to $FFFF.FFFF_{16}$.
- If no PCI bus device is installed, one of the following messages appears:

```
PMC 1/2 modules:
Error: Can’t set base-address of PMC1

PMC 1/2 modules:
Error: Can’t set base-address of PMC2
```

Example

In the following example a PMC module at PMC slot 1 is mapped to the PCI I/O space 0082.0000_{16} and to the PCI memory space 8000.0000_{16}. A user application can access the PCI bus device CSR registers via the PowerPC CPU at the PCI I/O space address $FE82.0000_{16}$ and at the PCI memory space address 8000.0000_{16}.

```
PowerBoot>
PowerBoot>
PowerBoot> PMCPCI 1 00820000 80000000

PMC1/2 modules:
PMC1, PCI address 0x00820000, Base Reg. 0x10, PCI I/O space, Master enable
PMC1, PCI address 0x80000000, Base Reg. 0x10, PCI MEM space, Master enable
Device ID = 0x0009; Vendor ID = 0x1011;
Status    = 0x0280; Command   = 0x0007;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x20;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x00;   Cache Line= 0x00;
base addr0= 0x00820001, base addr1= 0x80000000;
Max Lat   = 0x28;   Min Gnt   = 0x14;   IRQ Pin   = 0x01;   IRQ Line  = 0xFF;
Found PCI device: DEC Chip 21140A Fast Ethernet LAN


PowerBoot>_
```

5.3 RESET – Restarting the Board

The restarting of the CPU board via RESET is not as strong as a power-on reset. RESET incites only a jump to the /HRESET exception vector at $FFF0.0100_{16}$.

Syntax

```
RESET
```

Description

All devices based on the PCI bus will keep their PCI configuration space header region, e.g. the Ethernet controller will keep its default base address. But the shared memory, the PCI-to-ISA bridge, the serial console, the CIO parallel port, the Ethernet controller, etc. will be initialized. The L1 and L2 caches will be flushed and invalidated.

Example

```
PowerBoot> RESET
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller at address: 0xFE850000
Found PCI-to-PCI bridge at address: 0xFE860000
Found CPU740/750, PVR=00080202,
CPU clock: 251MHz, Bus clock: 83MHz, 8
DRAM EDO mode enabled, DRAM ECC mode enabled
Onboard DRAM      : none
Init DRAM Module 1:  16MB, 0x00000000..0x00FFFFFF
Init DRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 125MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board
Ethernet: 00:80:42:0E:1A:2E
Read DEC SROM...done - CRC is OK
PMC1/2: no auto mapping setup

<<PowerBoot V2.04 for PowerCore CPCI CPU-67X0>>

PowerBoot>
```

5.4 SETBOOT – Editing Auto Boot Parameters

SETBOOT prompts the user to enter values for the parameters required for the auto booting. The defined parameters become valid after the next power-on or when RESET is entered. The parameters are stored in the on-board NVRAM which keeps its contents during power-off and checks them after power-on or after RESET has been entered.

Syntax

SETBOOT

Description

After SETBOOT has been entered, the user is prompted to assign a value to each parameter described in the following. The prompt describes briefly the possible values of the respective parameters and the current setting.

The parameters described in the following

- define the location of the automatically loaded binary image: `boot select`
- determine the kind of booting and the location where the binary image is started: `auto boot`, `boot address`, `load address`
- select a delay for the auto booting after power-on: `auto boot delay`
- select one of the user flash devices: `boot user_flash`
- select a harddisk SCSI ID for booting a boot file: `boot disk SCSI ID`
- select a controller SCSI ID for a mounted PMC module: `PMCx controller SCSI ID`
- define the name and the path of the file loaded during auto boot: `TFTP/disk boot file name`
- select the internet protocol for connecting a server to the board: `RARP or ARP protocol`
- select the protocol numbers for selecting the TFTP file server and for identifying the board: `serverIP#`, `targetIP#`
- define the I/O or MEM address seen from the PCI bus which will be written to the PCI bus device of the PMC1 or the PMC2 module: `PMC1 PCI bus I/O base address` and `MEM base address`, same for PMC2

- define the I/O or MEM upstream and downstream base addresses, translated addresses, and setup base addresses which will be written into the PCI-to-PCI bridge:
  `Downstream CSR or I/O or MEM 0…3 BAR`
  `Upstream I/O or MEM 0…2 BAR`
  `Downstream I/O or MEM 0…3 Translated BAR`
  `Upstream I/O or MEM 0…1 Translated BAR`
  `Downstream I/O or MEM 0…3 Setup Register`
  `Upstream I/O or MEM 0…1 Setup Register`
- define whether the PCI-to-PCI bridge Primary Access Lockout bit is cleared after PowerBoot has initialized the board.

`boot select`
defines the location of the automatically loaded binary image:

– `0` = autoloads a binary image to `boot address` via Ethernet (TFTP and front-panel connector). The user must link the download application image to `boot address`.

– `1` = selects the user flash device preset by `boot user_flash`. Only 1 MByte of a user flash device can be mapped to the CPU at $\texttt{FFE0.0000}_{16}$ (paging). The execution is started at `boot address`.

– `6` = autoloads a PREP boot image from a SCSI harddisk as described in the PREP specification. If no PREP partition is found, a DOS 4.0 partition will be used. It is assumed that a PMC module is mounted at PMC1 or PMC2, which holds an NCR53C825 or an NCR53C875 SCSI 2 controller. The user has to prepare the harddisk format to be PREP compliant or DOS 4.0 compliant. Furthermore, the application image must be prepared for booting. If the partition format DOS 4.0 is used, the pure binary file to be booted can be copied from PC as normal DOS file to the root partition of the harddisk. The parameter `boot address` is used for downloading, `boot disk SCSI ID` for identifying the harddisk, `PMCx controller SCSI ID` is used for identifying the PMC based SCSI controller and `auto boot delay` for selecting a delay period after power-on.

– `7` = writes all parameters for the upstream and downstream windows to the PCI-to-PCI bridge. The primary lockout bit at the PCI-to-PCI bridge is set before the upstream and downstream parameters will be written. After this, the primary lockout bit will be cleared regardless of its status before auto booting.

– `8` = includes the same procedures as value `7` described above. Additionally, a binary image is autoloaded to `boot address` via Ethernet (TFTP and front-panel connector). The user must link the download application image to `boot address`.

– `9` = includes the same procedures as value `7` described above. Additionally, it selects the user flash device preset by `boot user_flash`. Only 1 MByte of a user flash device can be mapped to the CPU at $\texttt{FFE0.0000}_{16}$ (paging). The execution is started at `boot address`.

`auto boot`

enables or disables the auto booting.

– `0` = auto boot disabled. All NVRAM parameters are ignored. The PowerBoot debugger is invoked.

– `1` = auto boot enabled. Auto boot will take place after the next power-on or when `RESET` is used.

`auto boot delay`

selects a delay ranging from 0 to 99 seconds, i.e. this parameter delays the auto booting by a preset period of time. This is useful for example in case of spinning up a SCSI hard disk drive for booting. During count down of `auto boot delay` the auto booting can be stopped by pressing any user key on the serial console line.

`load address`

specifies the location in the CPU addressing space where the opcode is downloaded. `load address` does not depend on other NVRAM parameters. The binary image is always downloaded to `load address` by using the `boot select` parameters `0`, `3`, `6`.

`boot address`

specifies the location in the CPU addressing space where the opcode is started. It is independent of other NVRAM parameters. The binary image always starts at `boot address`, regardless, whether it is downloaded during power-on or stored in the user flash. For further information on the address map see section 5.1 “PPC/PowerCoreCPCI-6750 Address Map” on page 82.

`boot user_flash`

selects one of the four 8-bit wide organised user flash devices. The onboard logic of the PowerPC-to-PCI bridge provides only a 1-MByte sized window at the addressing space for user flash devices, even if the user flash devices are of 2-MByte size. Always the first MByte of a user flash device is mapped into a window (page 0). This window always ranges from $\texttt{FFE0.0000}_{16}$ to $\texttt{FFEF.FFFF}_{16}$ seen from the CPU addressing space. `boot user_flash` is used only

– if `boot select` is set to `1`

– and if `auto boot` is set to `1`.

In all other cases `boot user_flash` will be ignored and user flash 1 will always be preset after power-on.

`boot disk SCSI ID`
selects the harddisk SCSI ID for booting the harddisk. `boot disk SCSI ID` is set

– to `0` for harddisk drive 0,

– to `1` for harddisk drive 1,

– to `2` for harddisk drive 2, and so on.

`boot disk SCSI ID` can range between `0` and `15` and supports wide SCSI drives. `boot disk SCSI ID` is used only for the autoboot functionality. Other drives and their SCSI IDs may also be connected but they will be ignored during autobooting. SCSI parity checking is not supported.

`PMCx controller SCSI ID`
selects the SCSI controller ID for booting the harddisk. `PMCx controller SCSI ID` is set

– to `0` for SCSI ID 0,

– to `1` for SCSI ID 1,

– to `2` for SCSI ID 2 and so on.

`PMCx controller SCSI ID` can range between `0` and `15` and supports wide SCSI drives. `PMCx controller SCSI ID` is used only for the autoboot functionality. It may be changed on demand by an application software. SCSI parity checking is not supported.

IMPORTANT

The shared memory address range 0000.0000_{16}...0001.0000_{16} is used for CPU exception vectors and PowerBoot internals.

PowerBoot checks PMC1 and PMC2 for a mounted PMC module containing one of the following SCSI controllers:

– NCR53C825

– or NCR53C875

If one of the SCSI controllers mentioned above is found, it will be mapped automatically by firmware to the addresses shown in the following table.

Table 53 PCI I/O Addressing Spaces of the SCSI Controllers

PCI I/O addressing space	NCR53C825	NCR53C875
seen from the CPU	$FE82.0000_{16}$	$FE83.0000_{16}$
seen from the PCI bus	0082.0000_{16}	0083.0000_{16}

Other SCSI controllers are not supported and therefore they will be ignored.

`RARP or ARP protocol`
selects the internet protocol used for connecting a server to the board.

– `1` = selects RARP (Reverse Address Resolution Protocol). In case of RARP the parameters `serverIP#` and `targetIP#` are ignored.

– `2` = selects ARP (Address Resolution Protocol). In case of ARP the values entered for the parameters `serverIP#` and `targetIP#` are valid.

If another value is entered, the default setting `1` is assigned to the parameter.

`serverIP#`
defines the internet protocol number which selects the TFTP file server. If the internet protocol RARP is selected, `serverIP#` is ignored. `serverIP#` is stored as string, therefore it has to be written as shown in the following example *123.3.255.255*.

`targetIP#`
defines the internet protocol number identifying the board at internet layer. If the internet protocol RARP is selected, *`targetIP#`* is ignored. *`targetIP#`* is stored as string, therefore it has to be written as shown in the following example *3.255.37.67*.

`TFTP/disk boot file name`
defines the name and path of the file which will be loaded during auto boot (if `boot select` = `0`, `3`, or `6`). The file name including path is at most 128 characters.

If TFTP is used for booting, the host must be set up as TFTP server (`boot select` = `0` or `3`). The host has to be able to provide the desired file via Ethernet (TFTP and front-panel connector).

If a harddisk is used for booting (`boot select` = `6`), it must be set to the corresponding parameters defined by `boot disk SCSI ID`, `PMCx controller SCSI ID`, and `boot delay for SCSI disk`. At first the harddisk partitions 0 to 3 are scanned in order to find a PREP partition (41_{16}). If no PREP partition is found, a DOS 4.0-compatible harddisk partition (06_{16}) will be searched. In case of a valid DOS 4.0 partition, `TFTP/disk boot file name`

must be limited to a maximum of 8 characters followed by a dot `.` and an extension consisting of 3 characters (e.g. myfile.bin). All other names are ignored. Do not type a harddisk character like `C:\` in front of `TFTP/disk boot file name`. The root directory of the harddisk partition is searched only for `TFTP/disk boot file name`. Subdirectory levels are not searched and FAT32 systems are not supported.

In both cases (TFTP and harddisk) the user is fully responsible for upper case letters, lower case letters, and the file name itself.

`PMC`*`x`* `PCI bus` *`I/O or MEM`* `base address`
defines the respective I/O or MEM address based on the PCI bus device of the PMC*x* module.

The following description is divided into two parts:

– the first part is a general description of the PMC modules and their base addresses

– whereas the second part describes the 4 parameters.

On the PPC/PowerCoreCPCI-6750 up to 2 PMC modules can be installed. Every PMC module can have 2 different base addresses:

– one base address in the PCI bus I/O space

– and one base address in the PCI bus MEM space.

Depending on the features of the installed PMC modules, the addresses have to be set differently:

– If no PMC module is installed, set both addresses to `0`.

– If the installed PMC modules support only one addressing space, set the address which is not supported to $\texttt{FFFF.FFFF}_{16}$ to disable it.

– If the installed PMC modules support both addressing spaces, set both addresses to the desired value.

IMPORTANT

Do not set a PMC module base address to an address already used by the on-board PCI bus devices (see table 51 “PPC/PowerCoreCPCI-6750 Address Map Seen from the CPU” on page 82).

In the following the 4 parameters are described:

– `PMC1 PCI bus I/O base address`

– `PMC1 PCI bus MEM base address`

– `PMC2 PCI bus I/O base address`

– `PMC2 PCI bus MEM base address`

When defining the I/O base address of PMC*x*, the following is done:

– The PCI bus master bit (bit 2) is set to `1`.

– The PCI bus I/O space control bit (bit 0) is set to `1`.

– The value of the I/O base address is written to offset 10_{16}, which defines the first I/O base address register in the PCI device header type region.

When defining the MEM base address of PMC*x*, the following is done:

– The PCI bus master bit (bit 2) is set to `1`.

– The PCI bus MEM space control bit (bit 1) is set to `1`.

– The value of the MEM base address is written to offset 14_{16}, which defines the first MEM base address register in the PCI device header type region.

`OVERwrite Upstream/Downstream Setup Regs`

defines if the upstream/downstream setup registers are patched by NVRAM values. “1” enables the patching of the SROM downloaded setup register values by autoboot NVRAM based values. The setup register values given by the user later on, are used. “0” disables the patching of the SROM downloaded setup register values. The string expression “-NA-” will be shown instead of an user input line. No set-up register is changed or patched.

`Downstream CSR or I/O or MEM 0…3 BAR`

defines the base addresses written into the PCI-to-PCI base address register for the downstream windows 0, 1, 2, and 3. If `Downstream CSR I/O or MEM 0…3 BAR` is defined as 0000.0000_{16}, the respective window is disabled. Window 0 contains the CSR register set in the first 4-KByte of the memory space. Therefore, the minimum size of window 0 is 4 KByte. The remaining address space of window 0 can be set up into the MEM space. Window 1 can be set up into the I/O space or MEM space. Window 2 can be set up only into the MEM space. Window 3 consists of two 32-bit registers referred to as LOW and UP. These two 32-bit registers build one single 64-bit address located in the MEM space.

`Upstream I/O or MEM 0…2 BAR`
defines the base addresses written into the PCI-to-PCI base address register (BAR) for the upstream windows 0, 1, and 2. If `Upstream I/O or MEM 0…2 BAR` is defined as 0000.0000_{16}, the respective window is disabled. The window 0 can be set up in the I/O space or MEM space, whereas the windows 1 and 2 can be set up only in the MEM space.

`Downstream I/O or MEM 0…3 Translated BAR`
defines the base address written into the PCI-to-PCI translated base address registers 0, 1, 2, and 3. Accesses from the primary to the secondary side of the PCI-to-PCI bridge are translated into the address ranges in the registers.

`Upstream I/O or MEM 0…1 Translated BAR`
defines the base address written into the PCI-to-PCI translated base address registers 0 and 1. Accesses from the secondary to the primary side of the PCI-to-PCI bridge are translated into the address ranges in the registers.

`Downstream I/O or MEM 0…3 Setup Register`
defines the setup value written into the PCI-to-PCI setup register for the downstream windows 0,1, 2, and 3. `Downstream I/O or MEM 0…3 Setup Register` defines the size of the appropriate window.

`Upstream I/O or MEM 0…1 Setup Register`
defines the setup value written into the PCI-to-PCI setup register for the upstream windows 0 and 1. `Upstream I/O or MEM 0…1 Setup Register` defines the size of the appropriate window.

`Clear LOCKOUT bit`
defines if the PCI-to-PCI bridge LOCKOUT bit (bit 10) at the Chip Control 0 Register is cleared to 0 after booting procedure, or if it is left at the default power-on setting. The default power-on LOCKOUT bit setting is defined by hardware as 1. This setboot parameter is independent of all other setboot parameters stored in NVRAM and is checked after every reboot of the PPC/PowerCoreCPCI-6750. This parameter is introduced for PowerBoot Revisions V2.04 or higher.

IMPORTANT

If the CompactPCI system controller board in the Compact PCI rack does not seem to boot after power-on, the Primary Access Lockout bit of every PCI-to-PCI bridge located on the PPC/PowerCoreCPCI-6750 in every used CompactPCI I/O slot must be cleared. This prevents the CompactPCI system controller board from being stuck on endless PCI bus retry cycles while probing the CompactPCI bus configuration.

After the last parameter has been typed in, a checksum is calculated to protect the NVRAM contents from offset $1C00_{16}$ to $1FF0_{16}$ containing all edited parameters.

Example

```
PowerBoot>
PowerBoot> setboot

 -General boot parameters-

Boot select [0=Net, 1=Flash, 6=SCSI , 7=PCI, 8=PCI+Net, 9=PCI+FLASH] (0) :
Auto boot   [0=disable, 1=enable], (0)   :
Auto boot delay [0..99s], (0)   :
Load address (00000000) :
Boot address (00000000) :
Boot USER_FLASH [1..4], (1) :
Boot Disk SCSI-ID [0..15], (0) :
PMCx Controller SCSI-ID [0..15], (0) :

-TFTP Ethernet/Harddisk boot file parameters-

RARP [1] or ARP [2] protocol : (1) :
Server-IP# [aaa.bbb.ccc.ddd] : :
Target-IP# [aaa.bbb.ccc.ddd] : :
TFTP/Disk Boot file name :
:

 -PMC modul mapping parameters-

PMC1 PCIbus I/O base address (00000000) :
PMC1 PCIbus MEM base address (00000000) :
PMC2 PCIbus I/O base address (00000000) :
PMC2 PCIbus MEM base address (00000000) :


-PCI-to-PCI bridge Upstream/Downstream window mapping addresses-

OVERwrite Upstream/Downstream Setup Regs [0=disable, 1=enable],(0):

Upstream   I/O MEM 0 BAR        (00000000) :
Upstream       MEM 1 BAR        (00000000) :
Upstream       MEM 2 BAR        (00000000) :
Downstream CSR MEM 0 BAR        (00000000) :
Downstream I/O MEM 1 BAR        (00000000) :
Downstream     MEM 2 BAR        (00000000) :
Downstream     MEM 3 BAR LOW    (00000000) :
Downstream     MEM 3 BAR UP     (00000000) :
Downstream     MEM 0 Trans Base (00000000) :
Downstream     MEM 0 Setup Reg. (00000000) :-NA-
Downstream I/O MEM 1 Trans Base (00000000) :
Downstream I/O MEM 1 Setup Reg. (00000000) :-NA-
Downstream     MEM 2 Trans Base (00000000) :
Downstream     MEM 2 Setup Reg. (00000000) :-NA-
Downstream     MEM 3 Trans Base (00000000) :
Downstream     MEM 3 Setup L Rg.(00000000) :-NA-
Downstream     MEM 3 Setup U Rg.(00000000) :-NA-
Upstream   I/O MEM 0 Trans Base (00000000) :
```

```
Upstream   I/O MEM 0 Setup Reg. (00000000) :-NA-
Upstream       MEM 1 Trans Base (00000000) :
Upstream       MEM 1 Setup Base (00000000) :-NA-

-PCI-to-PCI bridge LOCKOUT bit setup-

Clear LOCKOUT bit [0=untouched, 1=clear], (0):
CSUM : 0x4A1
PowerBoot>
```

5.5 USERLED – Setting User LED

USERLED defines the color of the user LED at the front panel. The on-board user LED is red, green, or can be turned off.

Syntax

USERLED 1 or 2 *color*

color

defines the color of the user LED1 or 2:

- *red* = user LED U 1 or 2 is red
- *green* = user LED U 1 or 2 is green
- *dis* = user LED U 1 or 2 is off

Example

In the following example the user LED U is green:

```
PowerBoot> USERLED 1 green
PowerBoot> _
```

5.6 Flash Memory

PowerBoot enables you to easily program images into user flash memory devices.

5.6.1 Boot Flash

The boot flash device acts like a read-only device and cannot be reprogrammed by using a PowerBoot command.

5.6.2 User Flash

Since the size of a user flash window is defined as 1 MByte by the PowerPC-to-PCI bridge, every 2 MByte user flash memory device is divided into 2 pages. Page 0 accounts for the first MByte, page 1 for the

second MByte. In the future, 4 MByte user flash devices will have the additional pages 3 and 4.

The base address for every user flash device and for both of the pages within a user flash device is always $\texttt{FFE0.0000}_{16}$.

Erasing user flash devices

1. Start the PowerCoreCPCI-6750, PowerBoot V2.04.

```
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller at address: 0xFE850000
Found PCI-to-PCI bridge at address: 0xFE860000
Found CPU740/750, PVR=00080202,
CPU clock: 251MHz, Bus clock: 83MHz, 8
DRAM EDO mode enabled, DRAM ECC mode enabled
Onboard DRAM      : none
Init DRAM Module 1:  16MB, 0x00000000..0x00FFFFFF
Init DRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 125MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board
Ethernet: 00:80:42:0E:1A:2E
Read DEC SROM...done - CRC is OK
PMC1/2: no auto mapping setup

<<PowerBoot V2.04 for PowerCore CPCI CPU-67X0>>

PowerBoot>
```

2. Erase the user flash that you want to reprogram by using the `ferase` command. For example, if you want to erase user flash 1 type

```
PowerBoot> ferase user_flash1
Erasing flash memory ... done.
```

IMPORTANT

The `ferase` command erases the whole 2 MByte storage of the user flash device. If you only want to erase parts of the user flash device you need to use certain offset and length parameters. For a list of these parameters refer to the *PowerBoot User's Manual*.

IMPORTANT

PowerBoot first erases page 0 of the user flash device. It then automatically switches to page 1 and erases it. The switching cannot be seen by the user.

Loading an image into DRAM

3. In order to reprogram the user flash device you have just erased, you need to load the image into the DRAM memory first by using e.g. the `netload` command.

   Example:

```
PowerBoot> netload this-is-my-file-name 100000
   Init Ethernet Controller MII-Port and PHY-Device
   PHY-Device at 10MB/s negotiated
   LAN-controller at address FE850000 set to Ethernet 00:80:42:0E:00:69
   Transmitting RARP-REQUEST... Reception of RARP-REPLY
   Transmitting TFTP-REQUEST to server 02:80:42:0A:0D:79, IP 192.168.41.1
   PACKET:307 - loaded $00100000..$001265CF (157136 bytes)
   PowerBoot>
```

   As a second (principle) example, loading the word FORCE into page 0 of user flash 1 and COMPUTERS into page 1 of the same flash memory device, you need to type the following:

```
PowerBoot> bf 100000 200000 “FORCE” p
PowerBoot> bf 200000 300000 “COMPUTERS” p
```

4. Verify the DRAM memory contents by using the `md` command.

   Example:

```
PowerBoot> md 100000
00100000:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43 FORCE FORCE FORC
00100010:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100020:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100030:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
00100040:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100050:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100060:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
00100070:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100080:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100090:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
001000a0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
001000b0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
001000c0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
001000d0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
001000e0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
001000f0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
More (cr) ?
PowerBoot>
PowerBoot>
PowerBoot>
PowerBoot> md 200000
00200000:  43 4f 4d 50 55 54 45 52  53 20 43 4f 4d 50 55 54   COMPUTERS COMPUT
00200010:  45 52 53 20 43 4f 4d 50  55 54 45 52 53 20 43 4f   ERS COMPUTERS CO
00200020:  4d 50 55 54 45 52 53 20  43 4f 4d 50 55 54 45 52   MPUTERS COMPUTER
00200030:  53 20 43 4f 4d 50 55 54  45 52 53 20 43 4f 4d 50   S COMPUTERS COMP
00200040:  55 54 45 52 53 20 43 4f  4d 50 55 54 45 52 53 20   UTERS COMPUTERS
00200050:  43 4f 4d 50 55 54 45 52  53 20 43 4f 4d 50 55 54   COMPUTERS COMPUT
00200060:  45 52 53 20 43 4f 4d 50  55 54 45 52 53 20 43 4f   ERS COMPUTERS CO
00200070:  4d 50 55 54 45 52 53 20  43 4f 4d 50 55 54 45 52   MPUTERS COMPUTER
00200080:  53 20 43 4f 4d 50 55 54  45 52 53 20 43 4f 4d 50   S COMPUTERS COMP
00200090:  55 54 45 52 53 20 43 4f  4d 50 55 54 45 52 53 20   UTERS COMPUTERS
002000a0:  43 4f 4d 50 55 54 45 52  53 20 43 4f 4d 50 55 54   COMPUTERS COMPUT
002000b0:  45 52 53 20 43 4f 4d 50  55 54 45 52 53 20 43 4f   ERS COMPUTERS CO
002000c0:  4d 50 55 54 45 52 53 20  43 4f 4d 50 55 54 45 52   MPUTERS COMPUTER
002000d0:  53 20 43 4f 4d 50 55 54  45 52 53 20 43 4f 4d 50   S COMPUTERS COMP
002000e0:  55 54 45 52 53 20 43 4f  4d 50 55 54 45 52 53 20   UTERS COMPUTERS
002000f0:  43 4f 4d 50 55 54 45 52  53 20 43 4f 4d 50 55 54   COMPUTERS COMPUT
More (cr) ?
PowerBoot>
```

Programming the flash memory device

5. Program the image from the DRAM memory into the user flash device 1 by using the `fprog` command. The DRAM memory contents from $10.0000_{16}..1F.FFFF_{16}$ will be programmed into page 0 and $20.0000_{16}..2F.FFFF_{16}$ will be programmed into page 1.

   Example:

```
PowerBoot> fprog user_flash1 100000
Programming flash memory
0 ... 100%
Done.
```

6. Verify the programming session of the given user flash memory device 1 by using the `fselect` command.

   Example:

```
PowerBoot> fselect user_flash1
Base of flash window is 0xFFE00000
```

IMPORTANT

If you do not specify a page in the `fselect` command PowerBoot automatically selects page 0. To specify a certain page type the following:

Example:

```
PowerBoot> fselect user_flash1 0
```

for page 0

or

```
PowerBoot> fselect user_flash1 1
```

for page 1.

7. To see the contents of page 0 of the programmed user flash memory 1 use the `md` command.

   Example:

```
PowerBoot> md ffe00000
00100000:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
00100010:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100020:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100030:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
00100040:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100050:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100060:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
00100070:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
00100080:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
00100090:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
001000a0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
001000b0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
001000c0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
001000d0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f   E FORCE FORCE FO
001000e0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20   RCE FORCE FORCE
001000f0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43   FORCE FORCE FORC
More (cr) ?
PowerBoot>
```

Programming images of various sizes

PowerBoot enables you to program images that are

- smaller than 1 MByte
- smaller than 2 MByte
- larger than 2 MByte
- larger than 4 MByte

Images smaller than 1 MByte

To program images that are smaller than 1 MByte use the following command:

```
PowerBoot> fprog user_flash(x) source
```

IMPORTANT

Your image is programmed from offset 0 at page 0 until the end of your image. The remaining parts of page 0 and/or page 1 are programmed with random data from your DRAM memory. In order to program only the image, use the same command and additionally type the length of the specific file in hexadecimal numbers as an add-on parameter.

Images smaller than 2 MByte

To program images that are smaller than 2 MByte use the following command:

```
PowerBoot> fprog user_flash(x) source
```

IMPORTANT

Your image is programmed from offset 0 at page 0 until the end of page 0. PowerBoot then switches to page 1 and programs the rest of the image into page 1. The remaining parts of page 1 are programmed with random data from your memory. In order to program only the image, use the same command and additionally type the length of the specific file in hexadecimal numbers as an add-on parameter.

Images larger than 2 MByte

To program images that are larger than 2 MByte use the following commands:

```
PowerBoot> fprog user_flash(x) source
```

and

```
PowerBoot> fprog user_flash(x+1) source+20.0000(16)
```

IMPORTANT

Your image is programmed from offset 0 at page 0 of the first user flash device until the end of page 0. PowerBoot then switches to page 1 and programs it. The second command programs your image from offset 0 at page 0 of the second user flash device until the end of page 0. PowerBoot then switches to page 1 of the second user flash device and programs the rest of the image. The remaining parts of page 1 are programmed with random data from your memory. In order to program only the image, use the same 2 commands. Since the first user flash device is programmed with 2 MByte you need to type the residual length of the specific file in hexadecimal numbers after the second command. The residual length is the full length minus 2 MByte.

Example:

```
PowerBoot> fprog user_flash1 100000
PowerBoot> fprog user_flash2 300000
```

Images larger than 4 MByte

To program images that are larger than 4 MByte use the following commands:

```
PowerBoot> fprog user_flash(x) source
```

and

```
PowerBoot> fprog user_flash(x+1) source+20.0000_16
```

and

```
PowerBoot> fprog user_flash(x+2) source+40.0000_16
```

IMPORTANT

Your image is programmed from offset 0 at page 0 until the end of page 0. PowerBoot then switches to page 1 and programs it. Your image is then programmed from offset 0 at page 0 of the second user flash device until the end of page 0. PowerBoot then switches to page 1 of the second user flash device and programs it. Your image is then programmed from offset 0 at page 0 of the third user flash device until the end of page 0. PowerBoot then switches to page 1 of the third user flash device and programs the rest of the image. The remaining parts of page 1 are programmed with random data from your memory. In order to program only the image, use the same 3 commands. Since the first and the second user flash device is programmed with 2 MByte you need to type the residual length of the specific file in hexadecimal numbers after the third command. The residual length is the full length minus 4 MByte.

Example:

```
PowerBoot> fprog user_flash1 100000
PowerBoot> fprog user_flash2 300000
PowerBoot> fprog user_flash3 500000
```

Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

☞ Send this report to the nearest Force Computers headquarter listed on the address page.