GE Fanuc Automation

RM235

VME/PCMCIA

HARDWARE REFERENCE MANUAL

Document Number: Rx-URMH 086 Rev B

Embedded Systems

This page is intentionally left blank.

Notice

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, GE Fanuc Embedded Systems, Inc. assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

GE Fanuc Embedded Systems, Inc. reserves the right to make any changes, without notice, to this or any of GE Fanuc Embedded Systems, Inc. products to improve reliability, performance, function, or design.

GE Fanuc Embedded Systems, Inc. does not assume any liability arising out of the application or use of any product or circuit described herein; nor does GE Fanuc Embedded Systems, Inc. convey any license under its patent rights or the rights of others.

For warranty and repair policies, refer to GE Fanuc Embedded Systems, Inc. Standard Conditions of Sale.

Customer Care Support

Telephone: 1-800-GE FANUC or 434-978-5100
E-mail: support@gefanuc.com

1 Introduction

This manual describes operation, configuration and installation instructions for the RM235 VME/PCMCIA module. The RM235 is a VME to PCMCIA adapter with two independent blocks. Each block contains two PCMCIA sockets with ejectors to utilize up to 256 Megabyte of PCMCIA memory cards (FLASHs/EEPROMs/EPROMs/PROMs/SRAMs/OTP) or any PCMCIA I/O card, and is totally compatible with PCMCIA Release 2.1 and VME Rev.C1.

1.1 Features

- Operation Modes: Write, Read, Read - Modify - Write, Byte, Word, Longword, Block Transfer
- Address: A16 / A24 / A32
- Data: D08 / D16 / D32 (UAT)
- Addressing 4 Gigabytes
- Programmable selection of start and end address in 64K (10,000H)
- Control Status Programmable selection in 64K I/O address space
- Programmable to activate REG to read attribute memory mode for each block
- Programmable to activate +12V ,+5V and 3.3V
- Programmable for Interrupt and Interrupt Vector ID
- Programmable DTACK*
- Lifetime Warranty

2 Specifications

General specifications for RM235 are listed below.

CHARACTERISTICS	SPECIFICATIONS
Memory Capacity	Up to 256M Bytes
Address	A16, A24 or A32 Bits
Address Modifiers: 24 bits address	A24: Programmable
32 bits address	A32: Programmable
16 bits address (I/O)	A16: 29, 2D
24 bits address block transfer	A24: Programmable
32 bits address block transfer	A32: Programmable
Data	D08 / D16 / D32 (UAT)
Interface	VMEbus per REV.C1
Sockets	Two independent blocks. Each block can be used for different types of PCMCIA cards.
Socket Selection	Software selectable for start and end address in 64K (10,000H) boundaries for each block.
Control Status Register	Software selectable Write/Read to enable/disable +12V for FLASH, +5V, +3.3V or REG signals. Reports all batteries status and card detects.
I/O Selection	Selectable in 64K I/O address space.
Temperature: Operating	0°C to 65°C
Storage	-40°C to 85°C
Power Requirements	+5V @ 1.5A (typical), 1.8A max.

3 Hardware Installation

This chapter provides unpacking, hardware preparation and installation procedures for the RM235 module.

3.1 Unpacking Instructions

Unpack the RM235 module from shipping carton. Check and verify that all items are present by referring to the packing list. Reference the RM235 Component and Panel Front views on the following pages.

If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of equipment.

3.2 Handling

The RM235 uses MOS technology devices that are sensitive to static discharge. The memory module should never be plugged in or out of card cage while the power is applied to the module. The RM235 should be in an anti-static plastic bag or conductive foam for storage or shipment.

Note: Static discharge can damage circuit. Avoid touching areas of integrated circuitry.

3.3 Hardware Installation

To ensure proper operation of the RM235**,** all modifications can be made after installation. These modifications are made through Control Status Register (CSR) Address and all the registers are ***word access***.

Note: The write bits of the CSR are reset to zero on a powerup or reset.

The JMP1, JMP2, and JMP4 jumpers select the CSR address. The CSR can be mapped to any eight locations in 64K of VME short I/O address space.

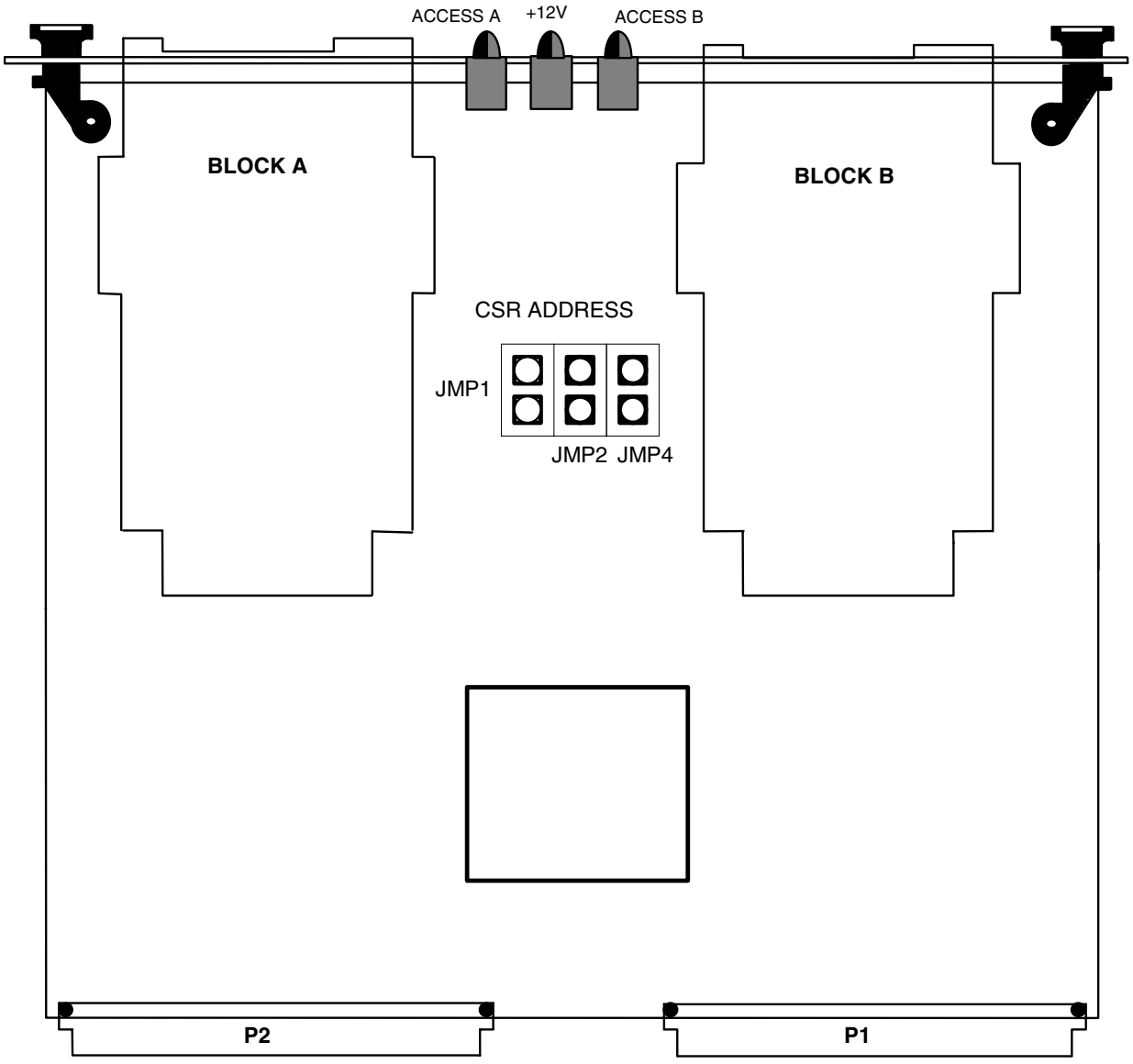
JMP4	JMP2	JMP1	I/O Address
0	0	0	0x1000
0	0	1	0x2000
0	1	0	0x3000
0	1	1	0x4000
1	0	0	0x5000
1	0	1	0x6000
1	1	0	0x7000
1	1	1	0x8000

Address 0x1000 factory default.

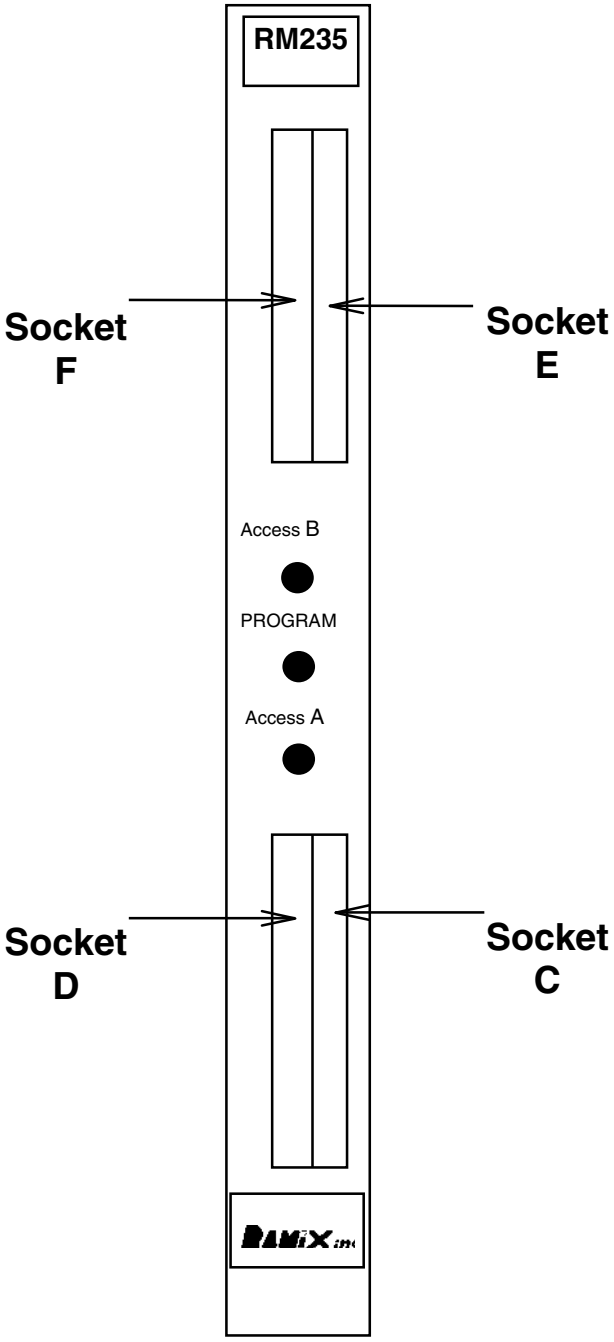
When a Jumper is installed the value is zero:

I/O Address Location = VME short I/O BASE Address Space + RM235 I/O SELECT

RM235 Component View


ACCESS A
+12V
ACCESS B
BLOCK A
BLOCK B
CSR ADDRESS
JMP1
JMP2 JMP4
P2
P1

RM235 Panel Front View



3.4 RM235 Installation

Turn all system power off. Carefully slide the RM235 module into the card slot. Be sure module is seated properly into DIN connectors on the back plane. Use screws to fasten module in chassis and turn system power on.

3.5 Operating

This section discusses the necessary information to use the RM235 module in a system configuration. This includes memory map, I/O map, status control, and indicators.

3.5.1 PCMCIA Socket Configuration

The RM235 has two Blocks A and B. Each block can be configured for different types of cards and each block consists of two sockets. Refer to the previous page to identify each socket.

3.5.2 CSR Register Description

The RM235 registers are described as follows:

Register Description	Registe Name	Relative Address (Hex)	Power on value	Data Bits
Block A Low Limit	R0	0 (R/W)	0x0000	D15..D0
Block A High Limit	R1	2 (R/W)	0x0000	D15..D0
Block B Low Limit	R2	4 (R/W)	0x0000	D15..D0
Block B High Limit	R3	6 (R/W)	0x0000	D15..D0
Address Modifiers: A32 Block, A32	R4	8 (R/W)	0x0000	D13..D8, D5..D0
Address Modifiers: A24 Block, A24	R5	A (R/W)	0x0000	D13..D8, D5..D0
Power	R6	C (R/W)*	0x0000	D15..D8
Configuration 0	R7	E (R/W)	0x0000	D15..D0
Configuration 1	R8	10 (R/W)	0x0000	D5..D0
Interrupt Requests	R9	12 (R/W)	0x0000	D14..D8,D6..D0
Interrupt ID0	R10	14 (R/W)	0x0000	D7..D0
Interrupt ID1	R11	16 (R/W)	0x0000	D7..D0
Interrupt ID2	R12	18 (R/W)	0x0000	D7..D0
Interrupt ID3	R13	1A (R/W)	0x0000	D7..D0
Status	R14	1C (R)	0x0000	D15..D0

*The low byte always reads zero.

All registers are ***word accessed*** and the undefined bits read zero (0). At power on, and reset all registers are set to zero.

3.6 VME Selection

The RM235 VME select can be accomplished by writing to R0 to R5. The R0 and R1 registers select the begin and the end address of the VME space for Block A. The R2 and R3 registers select the begin and end address of the VME space for Block B. The RM235 is designed to respond to either A24 or A32 address modifiers. Address Modifiers for A32 Block and A32 are set by R4. The address modifiers for Block A24 and A24 is set by R5.

VME Low Limit and High Limit registers R0, R1, R2 and R3 data bits correspond to the following address lines:

R0, R1, R2 & R3 Register Bit Description

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

The D015..D0 bits corresponds to A31..A16 address lines.

3.7 Address Modifiers (A24 or A32)

The RM235 is designed to respond to either A24 address modifiers or A32 address modifiers and is Software Programmable.

R4 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	AM5	AM4	AM3	AM2	AM1	AM0	0	0	AM5	AM4	AM3	AM2	AM1	AM0

R5 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	AM5	AM4	AM3	AM2	AM1	AM0	0	0	AM5	AM4	AM3	AM2	AM1	AM0

VME defines the following address modifiers, but any AM may be chosen as long as the processor is programmed with the same values:

Address Modifiers:	24 bits address	39, 3A, 3D and 3E
	32 bits address	09, 0A, 0D and 0E
	24 bits address block transfer	3B, 3F
	32 bits address block transfer	0B, 0F

3.8 Power Setting

The Vpp and Vcc for each socket are enabled independently by writing to the R6 register.

R6 Register High Byte

D15	D14	D13	D12	D11	D10	D9	D8
Vpp1 Socket F	Vpp1 Socket E	Vpp1 Socket D	Vpp1 Socket C	Vcc1 Socket F	Vcc1 Socket E	Vcc1 Socket D	Vcc1 Socket C

R6 Register Low Byte

D7	D6	D5	D4	D3	D2	D1	D0
Vpp0 Socket F	Vpp0 Socket E	Vpp0 Socket D	Vpp0 Socket C	Vcc0 Socket F	Vcc0 Socket E	Vcc0 Socket D	Vcc0 Socket C

The Vpp0 and Vpp1 in conjunction with each other have the following definition:

Vpp1	Vpp0	Vpp Voltage
0	0	0.0
0	1	+5.0
1	0	+12.0
1	1	High-Z

The Vcc0 and Vcc1 in conjunction with each other have the following definition:

Vcc1	Vcc0	Vcc Voltage
0	0	Forbidden
0	1	+3.3
1	1	+5.0
1	1	Forbidden

3.9 Configuration 0

The following table corresponds to the bit setting of the Configuration register zero.

R7 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7..D4	D3..D2	D1..D0
-REG Socket F	-REG Socket E	-REG Socket D	-REG Socket C	IOE Socket F	IOE Socket E	IOE Socket D	IOE Socket C	Reserved Write zero	Speed Block B	Speed Block A

The RM235 DTACK* signal is programmable for four different timings. Bit zero and bit one select timing for Block A. Bit two and three select timing for Block B. The bits are described as follows:

00 = 160 nsec
01 = 200 nsec
10 = 240 nsec
11 = 280 nsec

When the -REG is set for a socket access to the system memory window, it results in attribute memory on the PC Card accessed by asserting REG low. When set to 0, accesses to the system memory result in common memory on the PC card accessed by driving REG high.

Setting the IOE bit selects I/O PC Card, enabling the PC Card interface multi-plexer to route PC Card I/O signals. Setting the bit to 0 selects Memory PC Card.

The reserved bit always read zero and must be ***written zero.***

3.10 Configuration 1

The following table corresponds to the bit setting of the Configuration Register 1:

R8 Register

D15..D6	D5	D4..D0
0…00	Master INT Enb	Reserved

Setting Bit 5 enables the board to interrupt the VME. The reserved bits, D4..D0, read zero and must be ***written zero.***

3.11 Interrupt Request Lines

Each of the Blocks can interrupt the VME via any of the IRQ lines. The interrupt lines are programmable via Register R9. Following are the bit descriptions:

R9 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	IRQ 7 Blk B	IRQ 6 Blk B	IRQ 5 Blk B	IRQ 4 Blk B	IRQ 3 Blk B	IRQ 2 Blk B	IRQ 1 Blk B	0	IRQ 7 Blk A	IRQ 6 Blk A	IRQ 5 Blk A	IRQ 4 Blk A	IRQ 3 Blk A	IRQ 2 Blk A	IRQ 1 Blk A

When a bit is set, the PC Card interrupts on the corresponding VME IRQ. Only one bit for each block must be set.

3.12 Vector IDS

The RM235 responds to an 8-bit interrupt acknowledge cycle by providing an 8-bit vector ID on D0-D7. This ID is defined for each socket separately.

R10 Register

D15..D8	D7..D0
0…00	Vector ID Socket C

R11 Register

D15..D8	D7..D0
0…00	Vector ID Socket D

R12 Register

D15..D8	D7..D0
0…00	Vector ID Socket E

R13 Register

D15..D8	D7..D0
0…00	Vector ID Socket F

3.13 Status

The status register indicates the Battery Voltage (BV) and the Card Detect (CD) for each socket and it is a read only register.

R14 High Byte

D15	D14	D13	D12	D11	D10	D9	D8
Card Detect 2 Socket F	Card Detect 1 Socket F	Card Detect 2 Socket E	Card Detect 1 Socket E	Card Detect 2 Socket D	Card Detect 1 Socket D	Card Detect 2 Socket C	Card Detect 1 Socket C

R14 Low Byte

D7	D6	D5	D4	D3	D2	D1	D0
Battery Voltage 2 Socket F	Battery Voltage 1 Socket F	Battery Voltage 2 Socket E	Battery Voltage 1 Socket E	Battery Voltage 2 Socket D	Battery Voltage 1 Socket D	Battery Voltage 2 Socket C	Battery Voltage 1 Socket C

Each PCMCIA card has a two card detect signals (CD1, CD2) to provide proper detection of card insertion. When a card is inserted properly the CD1 and CD2 read as zero.

The battery voltage detect (BVD1, BVD2) is generated by the cards which use a battery (i.e., NVRAM) to indicate its condition. When both signals are kept asserted, the battery is in good condition. A replacement warning condition is signaled by BVD1 asserted and BVD2 negated, although data on the card is still assured. If

BVD1 is negated, the battery is no longer good and data is lost. The Battery Voltage status of each card is indicated by the Battery Voltage (BV) one and two. A good battery is indicated by the corresponding BV1 and BV0.

3.14 12V Indicator

The +12V FLASH indicator is on (yellow LED) when Vpp (+12V) is active.

3.15 Access Indicator

There are two ACCESS indicator LEDs, one for each block. When the [AS*] is low, an address matches the RM235 address decoding and the memory cycle is in progress.

3.16 I/O Cards

There are many I/O PCMCIA cards. The RM235 is capable of utilizing any of these cards. Some of these I/O cards are not 16-bit cards but are 8-bit cards.

3.17 Data Lines to Access Bytes

Since RM235 will provide 8, 16 or 32 bits of data, the relationship between the data lines and access byte locations are shown below.

D24-D31	D16-D23	D08-D15	D00-D07
BYTE(0)	BYTE(1)	BYTE(2)	BYTE(3)

BYTE(0) and BYTE(1) are connected to each BLOCK Socket D and F.

BYTE(2) and BYTE(3) are connected to each BLOCK Socket C and E.

4.0 Functional Description

This section provides the functional block diagram level description for the RM235 module.

4.1 General Information

The RM235 is a VMEbus PCMCIA module with options of accepting memory or I/O cards. The RM235 has two separate blocks. Each block is 32-bits wide for ROMs/PROMs/EEPROMs/EPROM/FLASH/SRAM or can be configured for 8-bits wide for different types of I/O cards, control status register to enable +12V FLASH programming mode, and A24/D32 or A32/D32 VMEbus interface.

4.2 Memory Access/Cycle Time

The RM235 access time from the VMEbus (activation of DS0*/DS1* to activation of DTACK*) is programmable. The cycle time depends on the number of clock periods required for the current VMEbus master to complete a VMEbus cycle.

4.3 Data Bus Structure

The RM235 is designed to accommodate the 8-bit, 16-bit, 32-bit, and unaligned transfer data bus structure. All data is latched during write/read access.

4.4 Address Counter

The RM235 has a 8-bit counter to be used in block transfer as 256. The counter will be loaded with an input address when AS* is low and address modifiers are for BLOCK transfer. The counter will then start counting with DS0*/DS1* (low to high) for either READ or WRITE cycles. At the end of block address strobe (AS*), it must be negated going high and asserted (AS* going low) with new addresses.

4.5 Software Issues

Some of the registers such as configuration register zero is shared by multiple sockets. In order not to change setup for other sockets, these registers must be read and the appropriate bits set/cleared and then rewritten.

When one PCMCIA card is inserted into a block the addresses are continuous (no skip in the address space). However, the access ***must be word wide***. When two cards are inserted into a block the addresses interleave between the two cards. The high word comes from one card and the low word comes from the second card. For example, if there is one Memory card in the socket and the memory card has the value of 1234 (hex) stored, when the memory is displayed we have the following:

```
01000000 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000010 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000020 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000030 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000040 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000050 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
01000060 1234  1234  1234  1234   1234  1234  1234  1234      .4.4.4.4.4.4.4.4
```

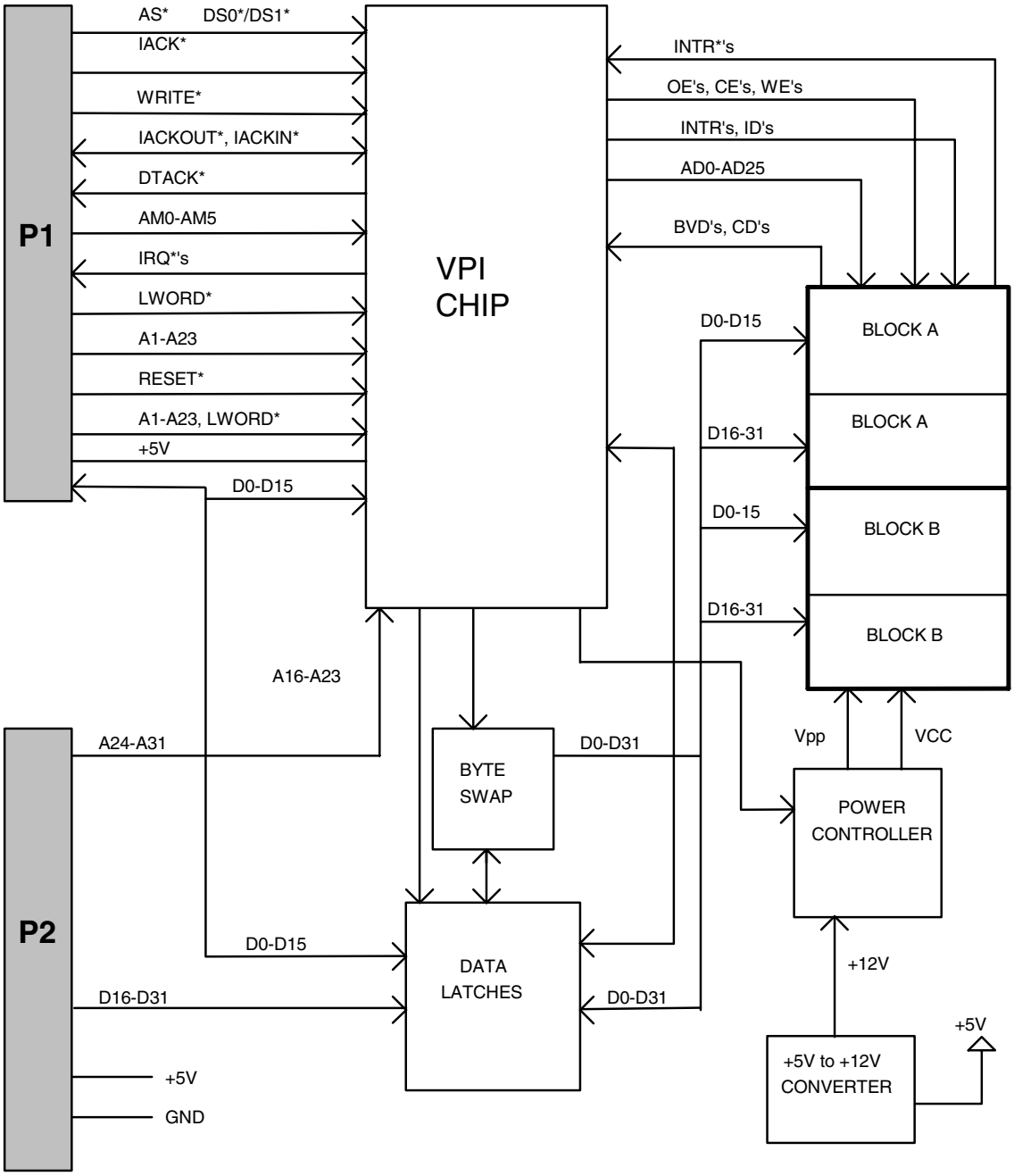
Assume now that the second memory card is inserted to the adjacent socket. If this memory card has the pattern 5678 (hex) and the memory is displayed we have the following (word and long access are shown):

```
01000000 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx
```

```
01000010 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx
01000020 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx
01000030 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx
01000040 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx
01000050 1234  5678  1234  5678   1234  5678  1234  5678      .4Vx.4Vx.4Vx.4Vx

01000000 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000010 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000020 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000030 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000040 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000050 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
01000060 12345678    12345678     12345678    12345678        .4Vx.4Vx.4Vx.4Vx
```

RM235 Functional Block Diagram



5.0 Support Information

This section provides the interconnection signals, and warranty information for the RM235 VME/PCMCIA module.

5.1 Interconnection Signals

The RM235 module interconnects with VMEbus through connector P1 with upper eight bits address and 16 bits data through connector P2.

5.1.1 Conncector P1 AND P2 Interconnection Signals

The RM235 memory module interconnects with VMEbus through Connector P1 and P2 (standard DIN triple-row, 96-pin male connector. The RM235 uses rows A, B, and C of P1 and row B of P2. Each pin connection, signal mnemonic, and signal characteristic for the connectors are identified in the Connector P1 and P2 Interconnect Signals tables on the following pages.

Connector P1 Interconnect Signals		
PIN No.	**SIGNAL MNEMONIC**	**SIGNAL NAME AND DESCRIPTION**
A1 - A8	D00-D07	DATAbus (bits 0-7) - Eight of 32 three-state bi-directional data lines.
A9	GND	GROUND - Connected to RM235 ground plane.
A11	GND	GROUND - Connected to RM235 ground plane.
A12	DS1*	DATA STROBE 1 - Signal that indicates which part of the data bus is transferring data. It is received by RM235 as a slave.
A13	DS0*	DATA STROBE 0 - Signal that indicates which part of the data bus is transferring data. It is received by RM235 as a slave.
A14	WRITE*	WRITE - Signal that specifies the direction of data transfer. It is received by RM235 as a slave.
A15	GND	GROUND - Connected to RM235 ground plane.
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - Signal that indicates that a valid data is available on the data bus during read cycle or that it has been accepted during write cycle. It is driven by the RM235 as a slave.
A17	GND	GROUND-Connected to RM235 ground plane.
A18	AS*	ADDRESS STROBE - The falling edge of this signal indicates that a valid address, address modifier, LWORD*, and IACK* are available on the VMEbus. It is received by the RM235 as a slave.
A19	GND	GROUND-Connected to RM235 ground plane.
A20	IACK*	INTERRUPT ACKNOWLEDGE IN - Signal that indicates an interrupt acknowledge cycle on the VMEbus. It received by the RM235.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of the three-state lines that provide additional information about the address bus, such as size, and cycle type. It is received by the RM235 as a slave.
A24 - A30	A07 - A01	ADDRESS bus (bits 7 - 1) - Seven of 31 three-state lines that specify an address in the memory map. It is received by the RM235 as a slave.
A32	+5V	+5 Vdc power - Used by the logic circuits and connected to the RM235 power (+5V) plane.
B4 - B5	BG0IN* -	BGO0UT* BUS GRANT IN AND BUS GRANT OUT (level 0) - Signals are bypassed through RM235.
B6 - B7	BG1IN* -	BG1OUT* BUS GRANT IN AND BUS GRANT OUT (level 1) - Signals are bypassed through RM235.
B8 - B9	BG2IN* -	BG2OUT* BUS GRANT IN AND BUS GRANT OUT (level 2) - Signals are bypassed through RM235.

Connector P1 Interconnect Signals		
PIN No.	**SIGNAL MNEMONIC**	**SIGNAL NAME AND DESCRIPTION**
B10 - B11	BG3IN* -	BG3OUT* BUS GRANT IN AND BUS GRANT OUT (level 3)- Signals are bypassed through RM235.
B16 - B19	AM0 - AM3	ADDRESS MODIFIER (bit 0 - 3) - Same as AM4 on pin A23
B20	GND	GROUND-Connected to RM235 ground plane.
B23	GND	GROUND-Connected to RM235 ground plane.
B32	+5V	+5 Vdc power - Used by the logic circuits and connected to the RM235 power (+5V) plane.
C1 - C8	D08 - D15	DATA bus (bit 8 - 15) - Same as D00 - D07 on pins A1 - A8.
C9	GND	GROUND - Connected to RM235 ground plane.
C11	BERR*	BUS ERROR - Signal driven by the bus master time-out circuit when it is the system controller and a VMEbus data strobe cycle exceeds 50 to 57 usec. The RM235 drives this signal if block transfer size exceeds its limit.
C12	SYSRESET*	SYSTEM RESET - Signal is an input to the RM235 to reset all of its devices.
C13	LWORD*	LONGWORD - Signal driven true (low) by the bus master when it does a 32-bit data transfer over the VMEbus. It is monitored by the RM235 to distinguish 32-bit from 16-bit data accesses to its memory from the VMEbus.
C14	AM5	ADDRESS MODIFIER (bit - 5) - Same as AM4 on pin A23.
C15 - C30	A23 - A08	ADDRESS bus (bits 23 - 08) - 16 of 31 three-state lines that specify an address in the memory map. They are received by the RM235 as a slave.
C32	+5V	+5 Vdc power- Used by the logic circuits and connected to the RM235 power (+5V) plane.

Connector P2 Interconnect Signals		
PIN No.	**SIGNAL MNEMONIC**	**SIGNAL NAME AND DESCRIPTION**
B1	+5V	+5 Vdc power - Used by the logic circuits and connected to the RM235 power (+5V) plane.
B2	GND	GROUND -Connected to RM235 ground plane.
B4 - B11	A24 - A31	ADDRESS bus (bits 24 - 31) - Eight of 31 three-state lines that specify an address in the memory map. It is received by the RM235 as a slave.
B12	GND	GROUND - Connected to RM235 ground plane.
B13	+5V	+5 Vdc power - Used by the logic circuits and connected to the RM235 power (+5V) plane.
B22	GND	GROUND - Connected to RM235 ground plane.
B23 - B30	D24 - D31	DATA bus (bits 24 - 31) - Eight of 32 three-state bi-directional data lines that provide the data path between VMEbus master and slave.
B31	GND	GROUND - Connected to RM235 ground plane.
B32	+5V	+5 Vdc power- Used by the logic circuits and connected to the RM235 power (+5V) plane.

Embedded Systems

GE Fanuc Embedded Systems Information Centers

Americas:
1-800-GE FANUC or (256) 880-0444

Asia Pacific:
+86 (10) 6561 1561

Europe, Middle East and Africa:
+33 (0)1 4324 6007

Additional Resources

For more information, please visit the
GE Fanuc Embedded Systems web site at:
www.gefanuc.com/embedded