Dy 4 Systems

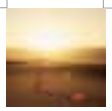
The future of high-integrity, embedded technology

SVME/DMV-179

PowerPC™ 750/7400 Single Board Computer with Dual PMC Interface

Features

- PowerPC™ 750 or 7400 (AltiVec Technology™-enhanced) CPU
- CPU core frequency up to 400 MHz
- 64, 128, or 256 Mbytes Synchronous DRAM with ECC without mezzanines
- 1 Mbyte (with 750 CPU) or 2 Mbytes (with 7400 CPU) of L2 cache
- Peak processor-memory bandwidth of 528 Mbytes/sec; peak L2 cache bandwidth of 1.064 Gbytes/sec
- Up to 48 Mbytes of 64-bit wide direct memory-mapped Flash memory
- 32 Kbytes of AutoStore nvSRAM
- 512 bytes of Serial EEPROM
- Two IEEE P1386/1386.1 64-bit, 33 MHz PMC sites for high-performance I/O expansion
- 64-bit PCI local bus architecture, 264 Mbytes/sec peak data transfer rate
- 10/100BaseTX (twisted pair) Ethernet™ port
- 8 or 16-bit Ultra SCSI interface
- Two EIA-232 serial ports
- Two HDLC/SDLC-capable EIA-422/485 serial channels, one with DMA support
- 12 bits of discrete TTL I/O, each with interrupt capability
- One 32-bit, three 24-bit general purpose timers
- Three 16-bit system timers
- Watchdog timer with software programmable time-out period
- Real Time Clock with automatic +5 V/+5 V STDBY switchover
- Four general-purpose PCI DMA controllers
- Tundra Universe II™ VME64 master/slave interface
- Comprehensive Foundation Firmware with:
  - debug monitor and non-volatile memory programmer;
  - suite of card support service routines;
  - BIT firmware with 95% fault coverage
- VxWorks® / Tornado BSP and Driver Suite (see separate data sheet for details)
- LynxOS™ reference port
- Occupies single .8" slot in all configurations
- Basecard card uses +5 V only, backplane 3.3 V, 5 V and ±12 V are routed to the PMC sites
- Supported by a staff of factory-based customer support specialists and a network of regional Field Application Engineers
- Available in a range of ruggedization levels, both air and conduction-cooled.



The SVME/DMV-179 continues the evolution of Dy 4's industry-leading MIL/rugged line of PowerPC™-based single board computers (SBC). Packed with features to satisfy the real-world requirements of defense/aerospace systems integrators, the SVME/DMV-179 is designed with performance, reliability, and ease of use in mind.

The '179 introduces a fully 64-bit architecture, a ground-breaking 48 Mbytes of direct memory-mapped, 64-bit wide Flash at a low power dissipation of only 17 Watts (typical with 750 CPU). Providing high-performance synchronous DRAM combined with the high system integrity of Error Checking and Correcting (ECC), the SVME/DMV-179 is ready for the challenges of avionics, tactical ground vehicle, and rugged naval applications.

For retrofit and technology insertion applications, the SVME/DMV-179 offers a common I/O feature set and the option of pin-out compatibility to earlier generations of Dy 4 PowerPC SBCs. As a member of Dy 4's continuously evolving stream of PowerPC SBCs, the SVME/DMV-179 supports the life-cycle model of successive technology insertions throughout a platform's life time.

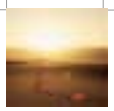
Architecture

Figure illustrates the SVME/DMV-179 architecture. The processor level 2 (L2) cache connects directly to the processor via the "backside" 64-bit L2 cache bus. A highly integrated bridge chip interfaces the PowerPC processor bus to the 64-bit PCI bus and acts as the memory controller. Via the bridge chip, the processor has access to the 48 Mbytes of 64-bit wide Flash, the 64-bit synchronous DRAM, and the 64-bit PCI bus. Up to 256 Mbytes of Synchronous DRAM are provided directly on the main board with no need for a mezzanine card. As well, the bridge chip provides extensive buffering via FIFOs. This allows the bridge chip to provide the processor data from SDRAM while simultaneously performing a burst read on the PCI bus.

The 64-bit, 33 MHz PCI bus provides a high-speed data path with which to access the VMEbus, 10/100 Mbit/sec Ethernet™ interface, Ultra SCSI, and the two expansion PMC sites. With a peak transfer rate of 264 Mbytes/sec, the PCI bus has the necessary capacity to support high bandwidth PMC modules such as Fibre Channel interfaces, display controllers, and custom high-speed interfaces.

Ever more complex application requirements and higher levels of software abstraction lead to larger and larger software loads. The SVME/DMV-179 meets this challenge with state-of-the-art technology that provides up to 48 Mbytes of non-volatile program and data storage.

The innovative use of high-efficiency switching regulators for the 3.3 V and CPU core requirements is integral to allowing all the functionality of the SVME/DMV-179 to be powered by only 17 Watts of +5 V power (typical, 750 CPU).



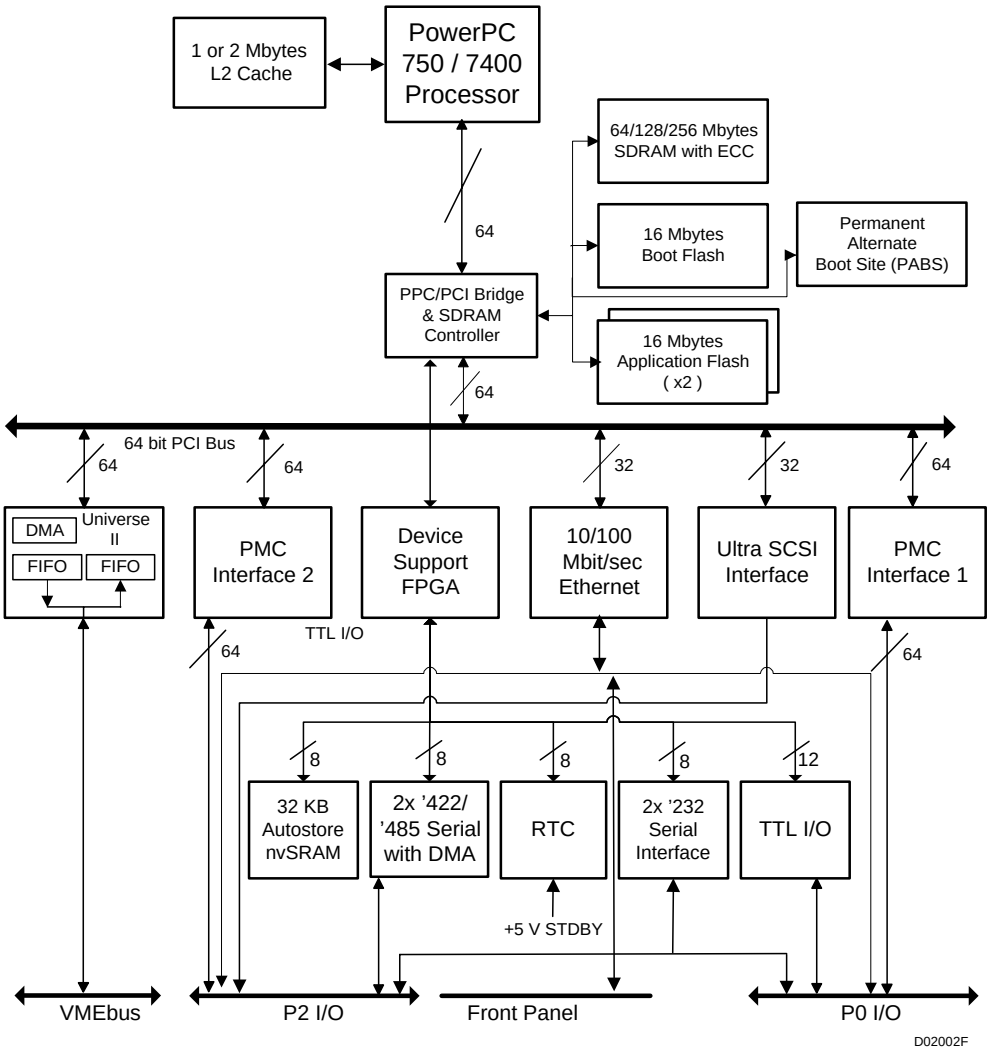


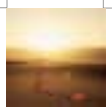
Figure 1: Block Diagram (see Table 3 for alternate I/O Routing)

Designed for Harsh Environments

All versions of the SVME/DMV-179 are functionally identical, with air-cooled versions available in Dy 4 ruggedization levels 0, 50, 100 and 200 and conduction-cooled versions in levels 100 and 200.

The conduction-cooled (DMV) version is designed for harsh airborne, land-mobile, and naval applications where circuit cards may be subjected to extremes of temperature, shock, vibration, and humidity. Dy 4's standard ruggedization guidelines define the environmental tolerance of each ruggedization level (see Ruggedization Guidelines data sheet for more information).

For thermal management, thermal layers within the PWB conduct heat away from the components, and an additional stiffening frame improves heat dissipation, plus shock and vibration resistance. Standard wedgelock fasteners ensure a reliable thermal and rigid mechanical connection to the chassis.



To ensure a long in-service life for the product, Dy 4 carefully analyses the projected fatigue life of all solder joints and interconnections. The mounting of all components is reviewed to ensure that differential thermal expansion between the component and the Printed Wiring Board (PWB) does not unduly shorten the fatigue life of the solder joints.

In the particular case of ceramic Ball Grid Array (BGA) components, studies have shown that the large difference in coefficient of thermal expansion between the ceramic package and typical PWB materials leads to early joint breakage after temperature cycling unless special mounting provisions are used. To solve this problem Dy 4 converts ceramic BGA components to Column Grid Array (CGA) components before soldering them to the board. The additional height of the column compared to a collapsed ball relieves temperature-induced stresses sufficiently to avoid premature fatigue failures. This approach was first pioneered and proven on Dy 4's SVME/DMV-178 PowerPC SBC.

PowerPC™ CPU

The SVME/DMV-179 can be equipped with either a Power PC 750 CPU or a Power PC 7400 CPU.

The PowerPC 750 CPU is a third generation member of Motorola®'s PowerPC family of high-performance, 32/64-bit RISC-based microprocessors. Developed for both desktop and embedded applications, the 750 provides industry-leading performance per Watt. The '179's PowerPC processor runs at speeds of up to 400 MHz on-chip and offers estimated CPU benchmarks as shown in Table 1.

For the many applications that need the numerical processing power of Motorola's AltiVec Technology™, the SVME/DMV-179 can be provided with the MPC 7400 CPU, a member of Motorola's G4 processor family. AltiVec Technology enhances the PowerPC architecture through the addition of a 128-bit vector execution unit. The vector unit provides for highly parallel operations, allowing for the simultanous execution of up to 16 integer operations or 8 floating point operations per clock cycle. At 400 MHz, this translates to a peak computational rate of 3.2 GFLOPS.

Table 1: Device Manufacturer's Estimated Performance

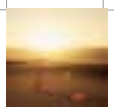
Processor	SPECint95	SPECfp95
750 at 400 MHz (1)	18.8	12.2
7400 at 400 MHz (2)	~19	~18.1

(1) Motorola 750 / 740 Fact Sheet, May 2000

(2) Motorola 7400 Fact Sheet, September 1999, derated to 400 MHz

L2 Cache

The SVME/DMV-179 provides 1 Mbyte of L2 cache (with 750 CPU) or 2 Mbytes of L2 cache (with 7400 CPU), implemented with synchronous burst RAM. Parity error detection is provided on the L2 data bus. At 133 MHz, the L2 cache bus is capable of a peak data transfer rate of 1.06 GBytes/sec.



DRAM

The main memory for the SVME/DMV-179 SBC is located entirely on the basecard with no need for extra mezzanine modules. The DRAM consists of either 64, 128, or 256 Mbytes of high performance synchronous DRAM (SDRAM). To preserve data integrity, the DRAM is provided with Error Checking and Correcting (ECC) circuitry that not only detects, but corrects all single-bit data errors, detects all double bit errors, and detects most errors of three bits or more. With ECC enabled, the peak data transfer rate to DRAM is 528 Mbytes/sec.

The DRAM is accessible from both the processor and the on-card PCI bus. Via the Universe II™ PCI-to-VME interface device, the DRAM is also accessible from the VMEbus.

Flash Memory

The SVME/DMV-179 has the capacity for up to 48 Mbytes of contiguous, directly-accessible, 64-bit wide Flash memory.

To minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical; '179 users can run user code directly from Flash without first cross loading to DRAM. This is practical due to the Flash memory's full 64-bit width and the fast access time of a 90 nsec.

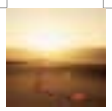
The Flash memory is implemented in three banks (0, 1, and 2) each of 16 Mbytes. The processor reset vector (0xFFF0_0100) is mapped to bank 0 which contains Dy 4's boot firmware. Banks 1 and 2 are intended for user application code. Two separate software write protect bits are provided for enabling Flash reprogramming. One controls the boot bank (bank 0) while the other controls the two application banks (banks 2 and 3) combined. To prevent inadvertant enabling, the two write protect bits are in separate registers.

This logical separation of boot and application Flash minimizes accidental corruption of the boot firmware when reloading application code into Flash. If desired, up to 14 Mbytes of the boot Flash can also be used for user code, at the expense of mixing boot firmware and user code into the same Flash bank.

Flash memory is reprogrammable on-board using either the Non-Volatile Memory Programmer utility (see *Non-Volatile Memory Programmer* data sheet) embedded into the standard foundation firmware, or Dy 4's FlashProg programming utility (see *FlashProg* data sheet). The Flash memory devices are specified for a minimum of 1,000,000 program-erase cycle and a data retention time of 20 years.

Permanent Alternate Boot Site (PABS)

The PABS provides a backup boot capability in the event that the foundation firmware in the main boot bank (bank 0) becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. The PABS provides users with a convenient mechanism to recover from corruption of the main boot bank without removing the card from the system in which it is installed. When a P0 backplane pin is asserted, the SVME/DMV-179 will boot from the PABS, and run a reduced-functionality version of Dy 4's General Purpose Monitor which can then be used to restore the main Flash.



AutoStore nvSRAM

The AutoStore nvSRAM provides fast, non-volatile storage of mission data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore nvSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss on the +5 V rail, an AutoStore cycle is performed and all 32 Kbytes are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an on-board capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 100,000 and the data retention period is 10 years.

Serial EEPROM

The SVME/DME-179 provides 512 bytes of Serial EEPROM for storing configuration data used by card initialization firmware. User access to the Serial EEPROM is also provided.

Ethernet™ Interface

An IEEE 802.3-compliant 10BASE-T/100BASE-TX Ethernet interface, implemented with a Symbios (LSI Logic) 53C885 SCSI/Ethernet device, is provided on the SVME/DMV-179.

On air-cooled cards the Ethernet interface is accessible from the front panel connector as well as on one or more backplane connectors. On conduction-cooled cards the Ethernet interface is accessible from backplane connectors only. A powerful chaining DMA controller and a 3 Kbyte FIFO for both receive and transmit channels ensures efficient utilization of the PCI bus and minimal processor loading.

SCSI-2 Interface

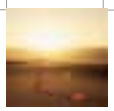
The SVME/DMV-179 comes standard with a single-ended, 8-bit Ultra SCSI (SCSI-2) interface, based on the Symbios (LSI Logic) 53C885 SCSI/Ethernet controller. This configuration is capable of peak transfer rates on the SCSI bus of 20 Mbytes/sec in synchronous mode, or 7 Mbytes/sec asynchronous.

The SVME/DMV-179 is also capable of providing Wide Ultra SCSI (SCSI-3) via a factory-set configuration option that brings out 8 extra SCSI data lines and the associated parity bit at the expense of serial channel 4 and the transmit clock of channel 3. In this configuration the device supports peak transfer rates of 40 Mbytes/sec synchronous and 14 Mbytes/sec asynchronous.

The SCSI controller of the 53C885 is highly autonomous and transfers data to and from SDRAM via an internal SCSI DMA controller and an associated 536-byte DMA FIFO, minimizing the loading of the main PowerPC processor by SCSI traffic. As a PCI master the 53C885 is capable of zero wait-state data bursts at 132 Mbytes/sec, conserving both PCI bus and main memory bandwidth.

EIA-232 Serial Ports

Two EIA-232 serial ports are provided based on an Exar 16C2550 controller chip. An input clock of 1.8432 MHz allows for programmable asynchronous baud rates from 50 baud to 115.2 Kbaud. The baud rate of each port can be set independently. The DSR signal on serial channel 1 is used as a cable detect signal to force the card to boot into the General Purpose Monitor.



On air-cooled cards the two EIA-232 channels are accessible on the front panel in addition to being available on the rear-panel on both air- and conduction-cooled cards.

EIA-422/485 Serial Ports

Two asynchronous and synchronous-capable EIA-422/485 ports are implemented via a Zilog 85C230 ESCC (Enhanced Serial Communications Controller). An input clock of 10 MHz provides for asynchronous communication at baud rates up to 153.6 Kbaud, and synchronous data rates up to 2.5 Mbps. To support high data rate applications without excessive loading of the PowerPC CPU, two of the general purpose DMA controllers provided by the bridge chip are available to the transmitter and receiver of serial channel 3.

To support multi-drop or half-duplex operation, the output drivers (clock and data) of each channel can be disabled. At power-up the output drivers are enabled for EIA-422 compatibility.

Discrete Digital I/O

The SVME/DMV-179 provides 12 bits of TTL-compatible discrete digital I/O. Each bit is individually programmable to be an input or output. In addition, each bit is capable of generating an interrupt upon a change of state, with the edge direction (high-to-low, low-to-high) also being programmable. On-board pull-up resistors are provided to allow direct connection to simple switch closure inputs. As outputs, the TTL discretes can sink 16 mA and source 12 mA.

Real-Time Clock (RTC)

The RTC function is provided by a Dallas Semiconductor DS1685 real-time clock chip. It contains registers for year, month, day, day-of-week, and seconds. The RTC is capable of periodic and alarm/wake-up interrupts to the CPU.

The RTC draws its power from the standard +5 V input during normal operation. In the event of loss of +5 V power, the RTC will automatically switch over to draw current from the +5 V STDBY line.

Timers

The SVME/DMV-179 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 2.

Watchdog Timer

The watchdog timer on the SVME/DMV-179 is a presettable downcounter with a resolution of 1 µsec. Time-out periods from 1 µsec to 16 seconds can be programmed. Initialization software can select whether a watchdog time-out causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog time-out log bit tells start-up code whether the last card reset was due to a watchdog time-out.

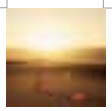


Table 2: Timing Resources

Timer Facility	Implementation	Type	Size	Tick Rate/Period	Maximum Duration
Time Base Register	PowerPC	Free running readable counter	64 bit	16.7 MHz/ 59.9 nsec.	35,033 years
Decrementer	PowerPC	Presettable, readable downcounter	32 bit	16.7 MHz/ 59.9 nsec.	257.2 sec.
General Purpose #0	Bridge chip	Presettable, readable downcounter with autoreload or stop options	32 bit	66.8 MHz/ 15 nsec.	64.3 sec.
General Purpose #1-3	Bridge chip	Presettable, readable downcounter with autoreload or stop options	24 bit	66.8 MHz/ 15 nsec.	251.6 msec.
RTC Periodic Interrupt	Real-time clock	periodic interrupt generator	-	from 122 usec. to 500 msec. by factors of two	500 msec.
Watchdog Timer	FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	24 bit	1 MHz/1 usec.	16.77 sec
System Timers #1-3	FPGA	Presettable, readable, cascadeable, downcounters with interrupt on terminal count	16 bit	1 MHz/1 usec.	65.5 msec. or 71.6 minutes when #1 and #2 are cascaded

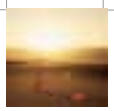
General Purpose DMA Controllers

Four DMA controllers provided by the bridge chip are available for general purpose use (two can be used to support DMA for serial channel 3). The four general purpose DMA controllers can be used for transferring large blocks of data between the SDRAM or Flash memory and PCI bus devices without loading down the PowerPC CPU. The General Purpose DMA controllers are capable of sustaining burst transfers using the full 64-bit width of the PCI bus. Advanced features include DMA chaining and the ability to schedule DMA transfers via a general purpose timer.

For transferring large blocks of data over the VMEbus, it is recommended that the DMA controllers internal to the Universe II device be used rather than the two general purpose DMA controllers. This is because the Universe II DMA controllers are capable of supporting maximum-size MBLT block sizes on the VMEbus.

VME Interface

The 64-bit PCI architecture of the SVME/DMV-179 combined with the Universe II's 64-bit PCI interface and extensive decoupling FIFOs allow for high-speed, bandwidth efficient data transfers between the VMEbus and on-board memory and PCI targets. VME data can be transferred at the full sustained rate of 50+ Mbytes/sec supported by the Universe II while only consuming only a fraction of the local PCI bus bandwidth of 264 Mbytes/sec.



Other key features of the SVME/DMV-179's VME interface include:

- Full system controller capability with support for both Dy 4/Tundra and VITA Auto-ID methods
- Programmable DMA controller with linked list support
- Wide range of VMEbus address and data transfer modes;
    - A32/A24/A16 master and slave, (not A64 or A40)
    - D64/D32/D16/D08 master and slave, (no MD32)
    - MBLT, BLT, ADOH, RMW, LOCK, and location monitors
- Four mailbox registers and four location monitors for inter-board communications and synchronization
- Nine programmable PCI-to-VME windows and four programmable VME-to-PCI windows
- Extensive support for Built-in-Test

The SVME/DMV-179 also provides support for five geographical addressing bits as defined by the ANSI/VITA 1.1-1997 (VME64 extensions) specification.

PCI Mezzanine Card (PMC) Expansion Sites

The functionality of the SVME/DMV-179 basic SBC can be substantially expanded via its two PMC sites. The two PMC sites interface to the basecard via the 64-bit, 33 MHz PCI bus, and interface to the outside world via 64-pins of back panel I/O per site. The placement of the PMC sites is such that a single, double width PMC module can also be fitted.

I/O routing is done in accordance with the IEEE P1386 specification, such that PMC 1's I/O is routed to the P0 connector while that of PMC site #2 is routed to the A and C rows of the P2. Front panel I/O is supported as a standard feature on air-cooled cards and, on a special order basis, for conduction-cooled cards.

For support of high-bandwidth PMC I/O signals such as Fibre Channel or digital video, both PMC site #1 and #2 are provided with four pairs of 150 ohm (nominal) differential impedance traces matching the PMC-642A1 pin-out. Trace length is equalized within pairs.

Conduction-Cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interface follows the VITA 20-200X Conduction Cooled PCI Mezzanine Card draft standard. To optimize the thermal transfer from PMC modules to the base card the standard DMV-179 thermal frame incorporates both the Primary and Secondary thermal interfaces as defined by VITA 20-200X. See Figure 2 for a sketch of the standard thermal frame.

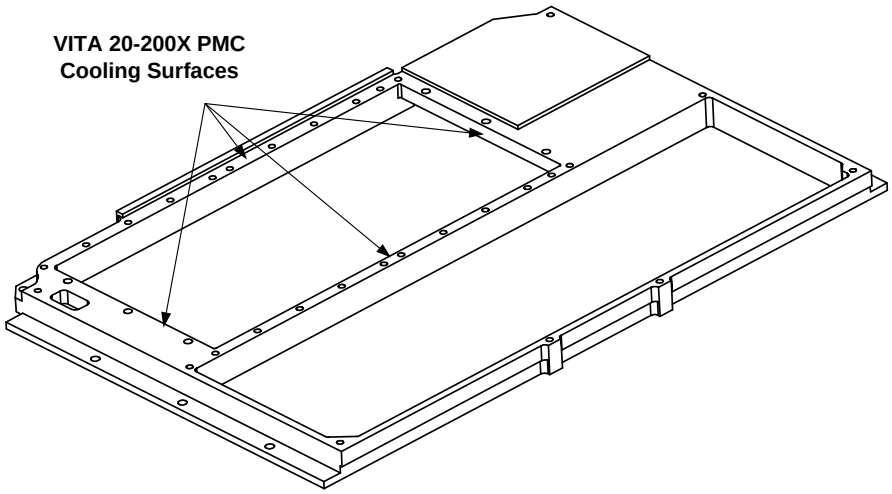


Figure 2: Thermal Frame with VITA 20-200X PMC Cooling Surfaces

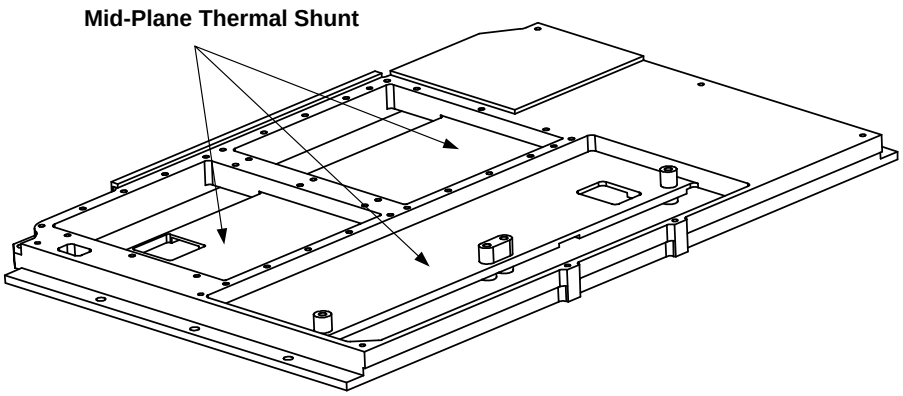


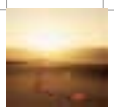
Figure 3: Thermal Frame with VITA 20-200X PMC Cooling Surfaces and Mid-Plane Thermal Shunt

High-power PMC Modules

To optimize the cooling of high-performance, high power PMC modules such as Dy 4's PMC-700 graphics module, an alternate thermal frame is available for the DMV-179 that incorporates a mid-plane thermal shunt as illustrated in Figure 3. High power PMC's can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the DMV-179 card edge to the PMC components. The mid-plane thermal shunt does not impinge on the VITA 20- specified component height.

PMC Power Routing

The PMC sites are provided with 3.3 V power from the VMEbus backplane — no 3.3 V power is provided by the SVME/DMV-179 itself.



PCI Signalling

The SVME/DMV-179 PCI bus uses 5 V signalling and is compatible with PMC modules that use 3.3 V signalling. The PMC sites are keyed as 5 volt sites.

Status Indicators and Controls

The SVME/DMV-179 SBC provides run/fail status by asserting a signal on the P0 connector and illuminating the red front panel LED in the event the diagnostics detect a card failure. There is also a software controlled green LED that the application can use to indicate status.

A card reset signal is available on the P0 connector and on the front panel connector on air-cooled cards. The front panel and P0 break-out cables for the SVME-179 include a push button switch that interfaces to this signal to allow the card to be reset without doing a full system reset.

JTAG and COP Test and Debug Interfaces

To support factory acceptance testing, the SVME/DMV-179 provides a JTAG scan chain port on the P0 connector that interfaces to those devices that support JTAG, such as the VMEbus interface chip, L2 cache, bridge chip, and others.

The PowerPC Control and Observation Port (COP) interface is accessible via the front panel on air-cooled cards and via copper pads on conduction-cooled cards. The COP interface is useful for software debug using a workstation tool such as EST's visionICE emulation system.

I/O Routing Options

To facilitate retrofit and technology insertion, the SVME/DMV-179 offers a common I/O feature set and the option of pin-out compatibility with earlier generations of Dy 4 PowerPC SBCs. Table 3 shows the I/O routing for the SVME/DMV-179 in its native ('178-compatible) mode as well as '176/177 compatibility modes.

Low Power Consumption

The application of advanced design techniques such as switching regulators for the 3.3 V and CPU core voltage requirements and maximum use of low power devices provides a low typical power of only 17 Watts for a fully populated card (without PMC modules, with 750 processor).

Power Routing

The SVME/DMV-179 basecard uses only +5 V and optionally +5 V STDBY. On-board regulators provide all necessary internal voltages. PMC sites are fed with +5 V, ±12 V, and 3.3 V directly from the backplane.

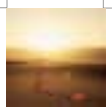
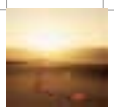


Table 3: I/O Routing Options

Mode	Description	Front Panel (air cooled cards only)	P0 Connector	P2 Rows A & C	P2 Rows D & Z
#1	Standard '178/'179 VME64x Configuration (5-row P1/P2, 95-pin P0)	- 2x EIA-232 - Ethernet - JTAG/COP interface - external card reset in	- PMC Site #1 I/O - 1x EIA-232 - discrete digital I/O - cardfail status out - external card reset in - JTAG test chain	- PMC Site #2 I/O	- Ethernet - SCSI (8-bit) - 2x EIA-232 - 2x EIA-422
#2	Optional '176/'177 P0/P2 Compatibility Mode (See Note 1) (See Note 2)	- 2x EIA-232 - JTAG/COP interface - external card reset in	- Ethernet - SCSI (8-bit) - 2x EIA-232 - 2x EIA-422 - discrete digital I/O - cardfail status out - external card reset in - JTAG test chain	- PMC Site #2 I/O	- Ethernet - SCSI (8-bit) - 2x EIA-232 - 2x EIA-422
#3	Optional '176/'177 P2-only Compatibility Mode (See Note 1) (See Note 2)	- 2x EIA-232 - JTAG/COP interface - external card reset in	- P0 connector not installed	- Ethernet - SCSI (8-bit) - 2x EIA-232 - 2x EIA-422 - cardfail status out	- Ethernet - SCSI (8-bit) - 2x EIA-232 - 2x EIA-422
#4	Optional 16-bit SCSI Mode (See Note 1)	- 2x EIA-232 - Ethernet - COP interface - external card reset in	- PMC Site #1 I/O - 1x EIA-232 - discrete digital I/O - cardfail status out - external card reset in - JTAG test chain	- PMC Site #2 I/O	- Ethernet - SCSI (16-bit) - 2x EIA-232 - 1x EIA-422 (no TxClk)

Note 1: Optional I/O routings are controlled by factory-set configuration links. Boards with other than the standard routing are built to order and set-up charges may apply.

Note 2: In all modes, the SVME/DMV-179 is equipped with 5-row P1 and P2 connectors.



Mechanical Format

Conduction-cooled modules conform to the dimensions defined in IEEE 1101.2-1992, Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards.

Air-cooled modules conform to the dimensions defined in ANSI/VITA 1-1994, American National Standard for VME64. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).

For air-cooled applications where the enclosure is not compatible with the IEEE 1101.10-style front panels, traditional-style front panel kits can be purchased separately for customer installation.

Foundation Firmware and BIT

The SVME/DMV-179 SBC is equipped with a comprehensive on-board firmware package called Foundation Firmware that includes:

- General Purpose Monitor (GPM) - provides low-level monitoring and debug functions to facilitate system startup and integration activities (see General Purpose Monitor data sheet for more information)
- Built-in-Test (BIT) – a library of Card Level Diagnostic (CLD) routines is provided to support Power-up BIT (PBIT), Initiated BIT (IBIT) and Continuous BIT (CBIT) (see Card Level Diagnostics data sheet for more information)
- Card Support Services (CSS) - provides a common software interface to the hardware features of the card (see Card Support Services data sheet for more information)
- Execution Sequencer (ES) - controls the invocation order of the software configuration items on the card (see Execution Sequencer data sheet for more information)
- Non Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of Flash memory (see Non-Volatile Memory Programmer data sheet for more information)

Dy 4's BIT firmware is designed to provide 95% fault coverage for testable functionality and supports tests in Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) modes. PBIT consists of a reduced set of tests that provide confidence that the hardware is operating correctly while minimizing power-up time.

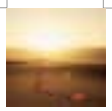
The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an off-line mode. CBIT allows applications to test hardware components in the background while the mission software operates as a higher priority task. The selection of tests for PBIT, IBIT, and CBIT is configurable.

Operating System Software

The SVME/DMV-179 is supported by the following real-time operating systems:

- VxWorks® (Tornado™) from Wind River Systems (see separate VxWorks BSP and Driver Suite data sheet for details)
- LynxOS™ from Lynx Real-Time Systems

Contact your Dy 4 representative for updates on support for other operating systems.



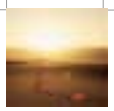
Integration Support

Dy 4 provides all the supporting items necessary to ensure a smooth system integration process. These include:

- Comprehensive hardware, firmware, and software documentation package, in hard copy and on CD-ROM
- Break-out cables for the front and rear-panel I/O to convert the '179-specific pin-outs to industry standard connectors for use in laboratory development environments
- FlashProg Flash memory programming facility (see *FlashProg* data sheet for more information) that simplifies the loading of user code into the SVME/DMV-179

Table 4: SVME/DMV-179 Specifications

RUGGEDIZATION LEVELS (Refer to *Ruggedization Guidelines* data sheet for more details)		
SVME card	Available in levels 0, 50, 100 and 200*	
DMV card	Available in levels 100 and 200*	
*For the SVME/DMV-179 level 200 temperature is -40°C to +85°C.		
POWER REQUIREMENTS		
	Maximum	Typical
+5 V (750) (+5.0%, -2.5%)	4.2 A	3.4 A
+5 V (7400) (+5.0%, -2.5%)	5.2 A	4.2 A
+12 V	0 A	0 A
-12 V	0 A	0 A
3.3 V	Only routed to the PMC sites, not used by the base card.	
+5 V STDBY: - with +5 V present - without +5 V	<1 uA 350 uA	<1 uA 300 uA
DIMENSIONS		
	Size	Weight
SVME card	per ANSI/VITA 1-1994	<500 g (<1.21 lbs.)
DMV card -standard thermal frame	per IEEE 1101.2	<600 g (<1.32 lbs)
DMV card - thermal frame with mid-plane thermal shunt	per IEEE 1101.2	<750 g (<1.65 lbs)



The information in this document is subject to change without notice and should not be construed as a commitment by Dy 4 Systems Inc. While reasonable precautions have been taken, Dy 4 Systems Inc. assumes no responsibility for any errors that may appear in this document.

References to other documents of the exact issue, or if not shown, the issue in effect at the time of publication form a part of this specification to the extent referenced herein. In the event of a conflict, this specification will be considered a superseding requirement.

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